A General Purpose Automatic Overlapped Tiling Technique in Polyhedral Frameworks

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Outline

Introduction to Tiling Techniques [IT88]

```
for (t=0; t<T; t++)
    for (i=1; i<N-1; i++)
        A[t+1][i]=0.25*(A[t][i+1]+2.0*A[t][i]+A[t][i-1]);
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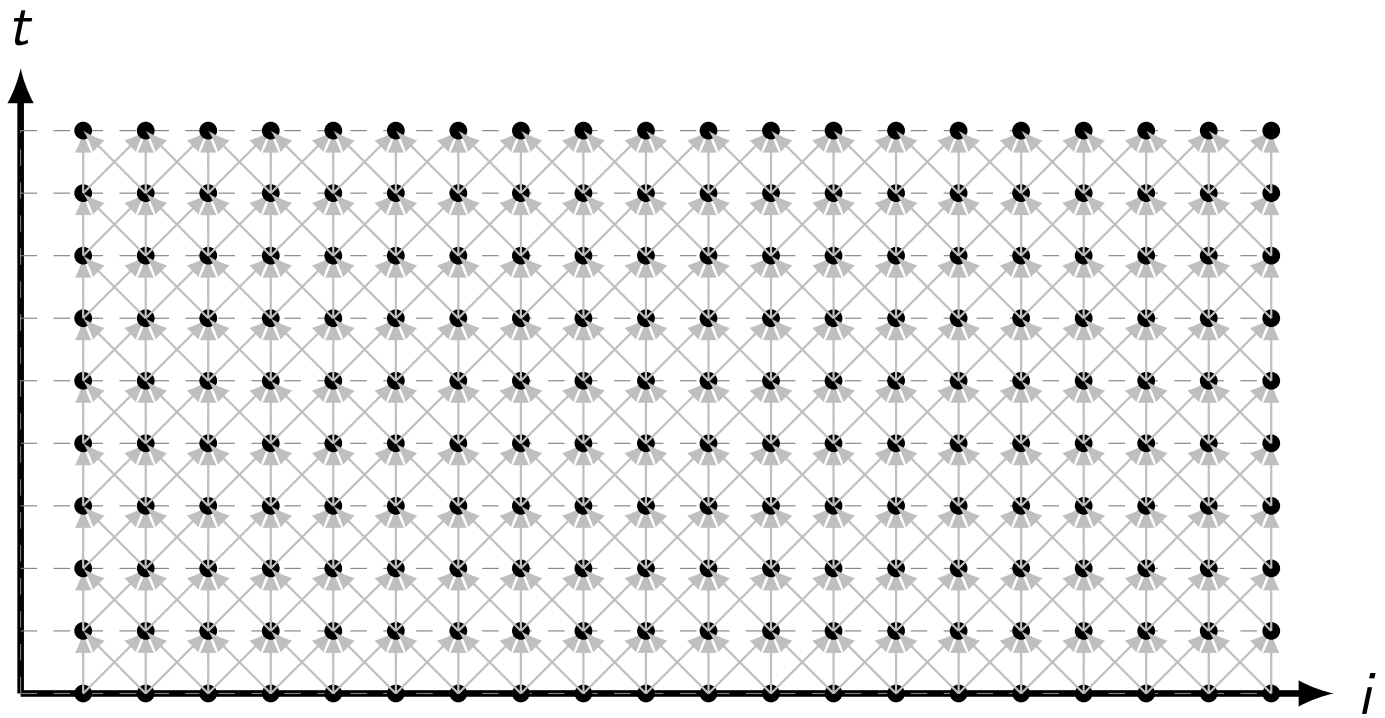
Stencil Code from heat-1d.c



Different tile shapes on the above stencil code's iteration space

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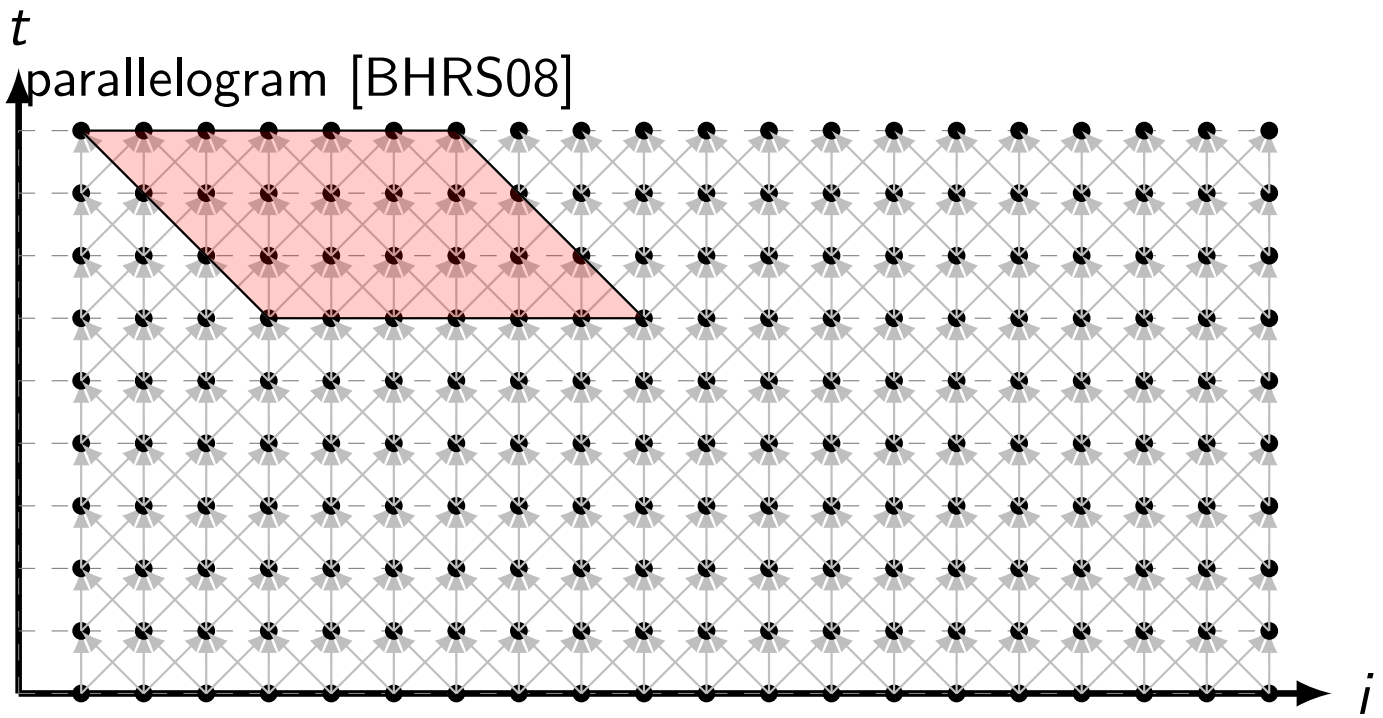

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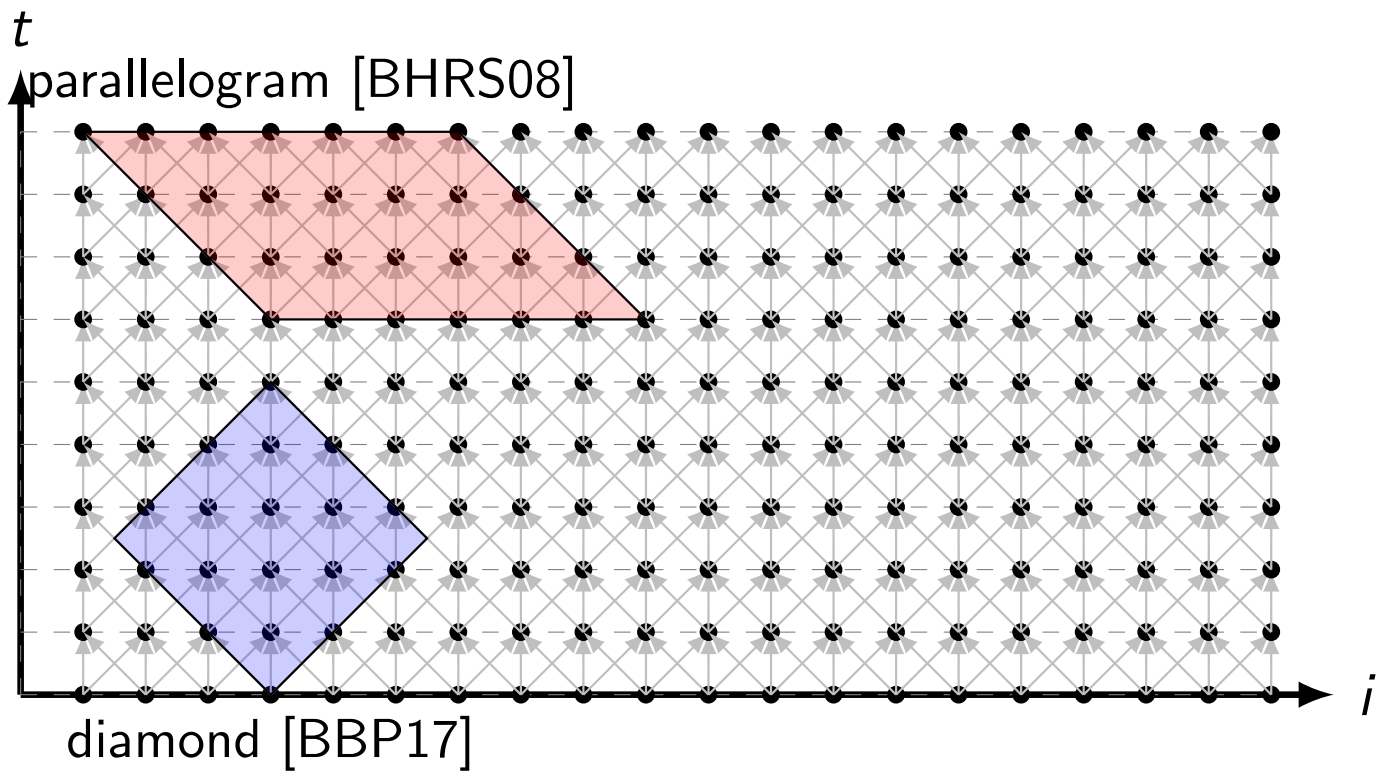

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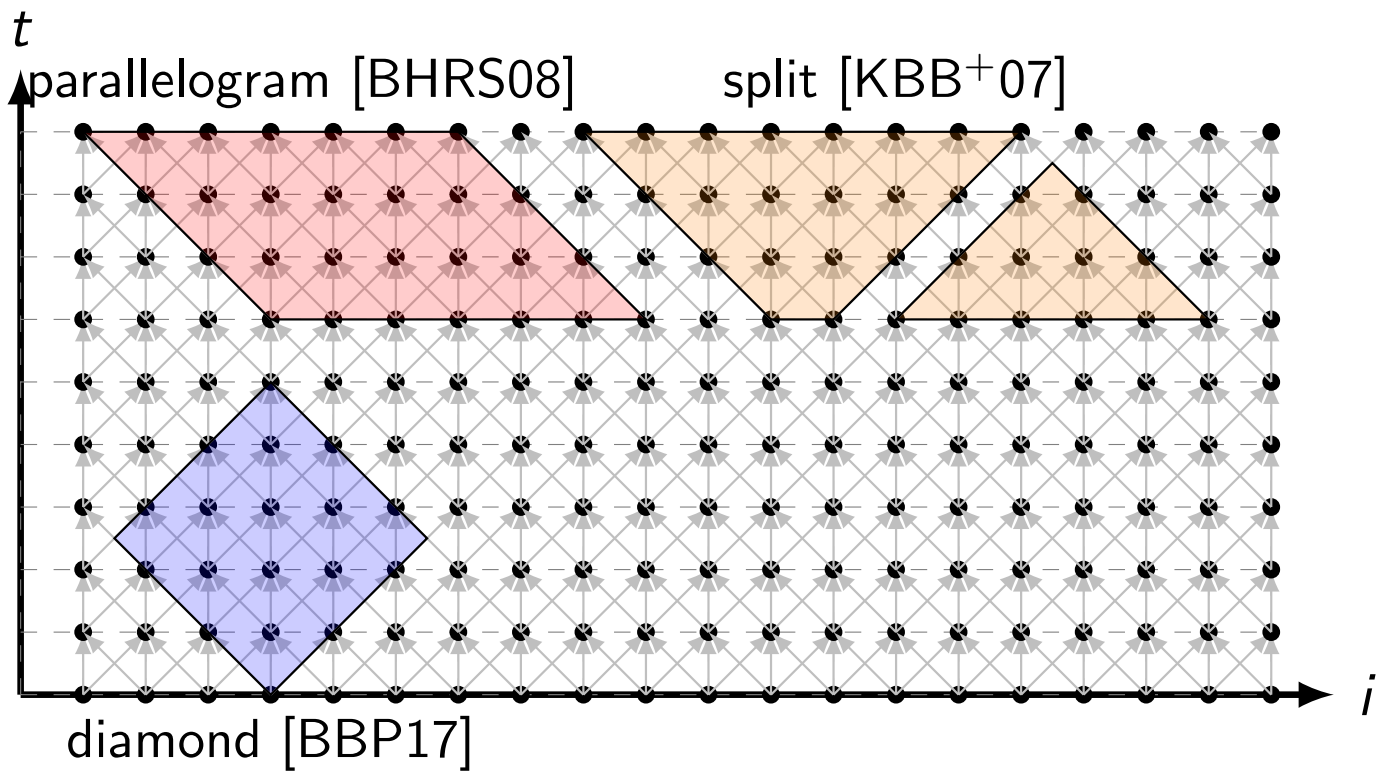

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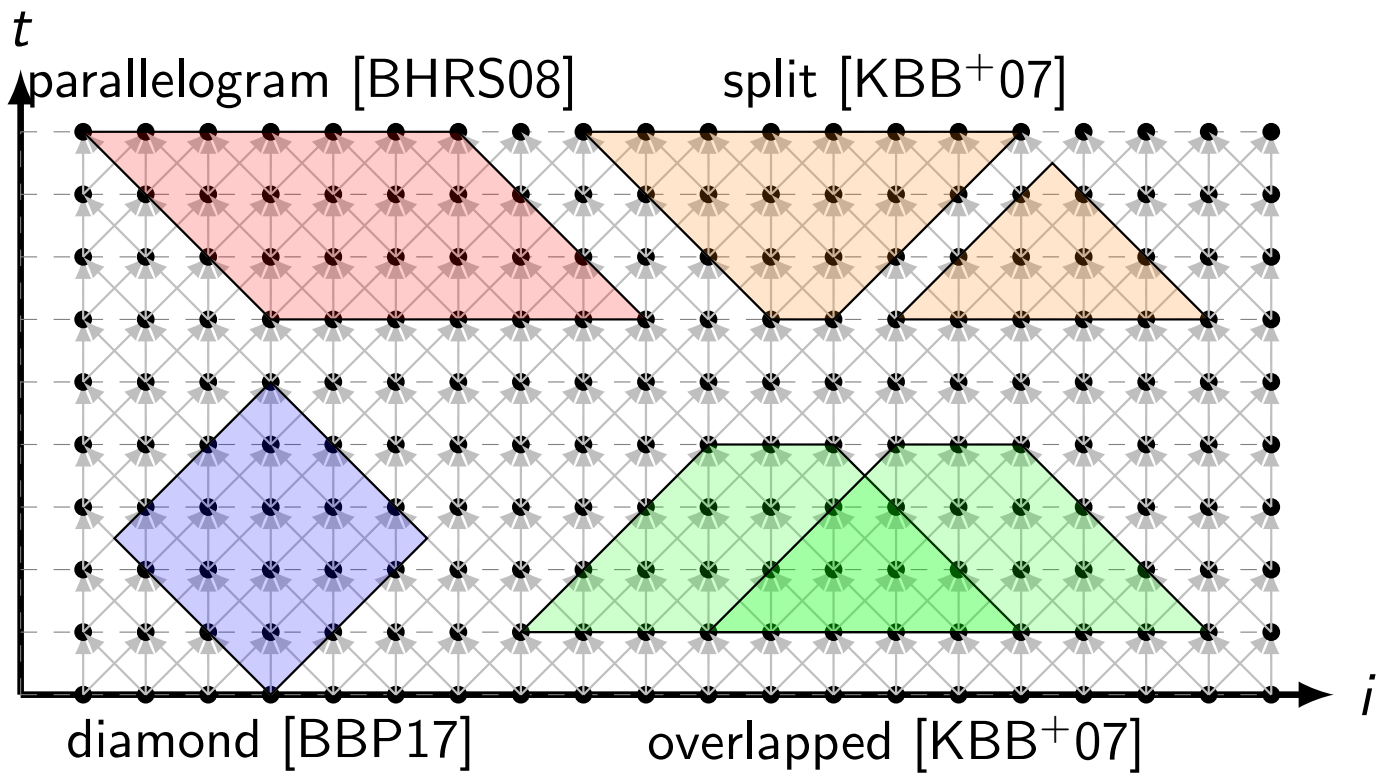

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Comparison Between Different Tiling Techniques

	parallelogram	diamond	split	overlapped
shape complexity	×	✓	✓	✓
parallelism	×	✓	✓	✓
locality	✓	✓	✓	✓
redundancy	×	×	×	✓
algorithmic complexity	×	✓	✓	×

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  - Overlapped tiling

Comparing with PolyMage

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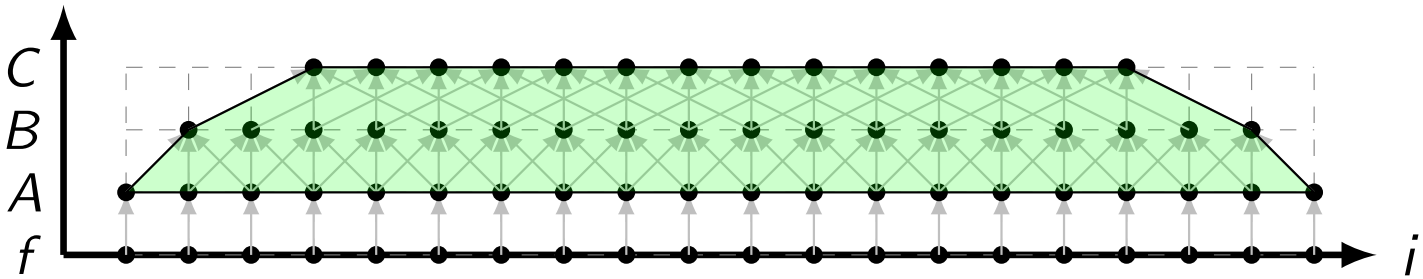
A simple image processing pipeline



Overlapped tiling on the iteration space

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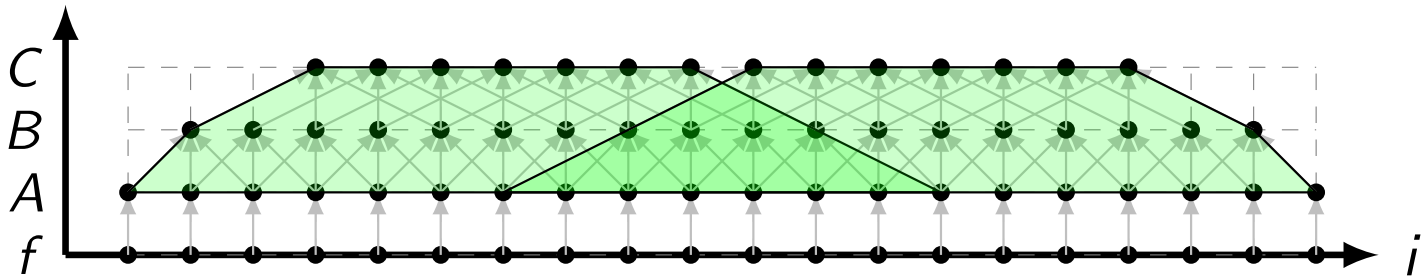

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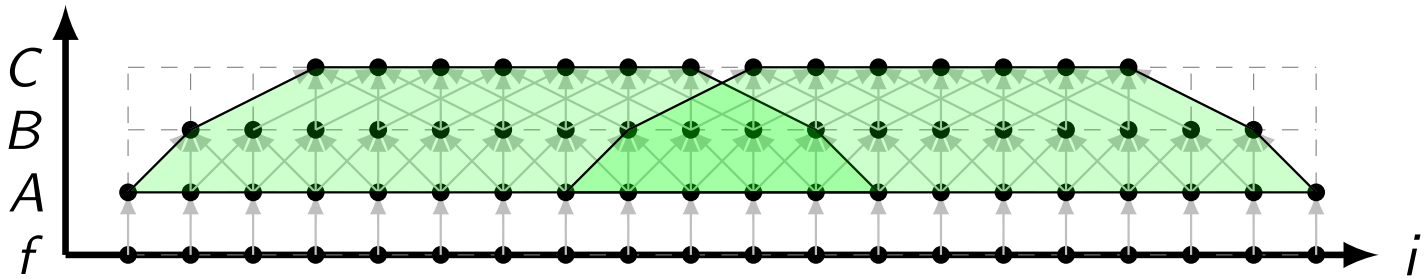

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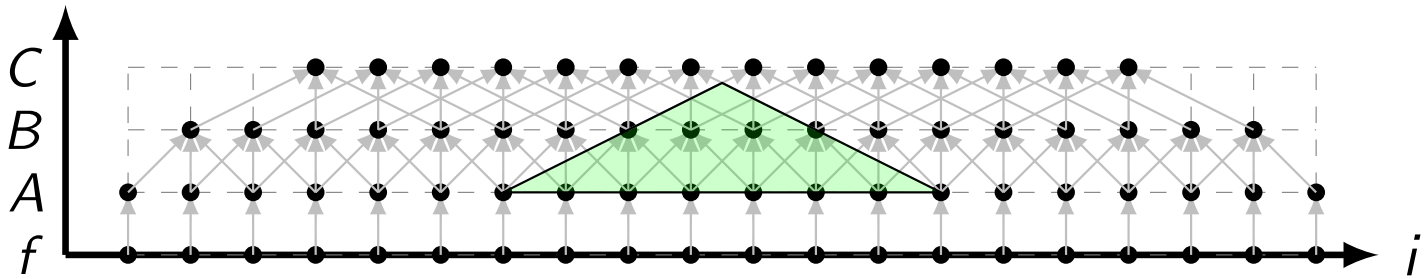

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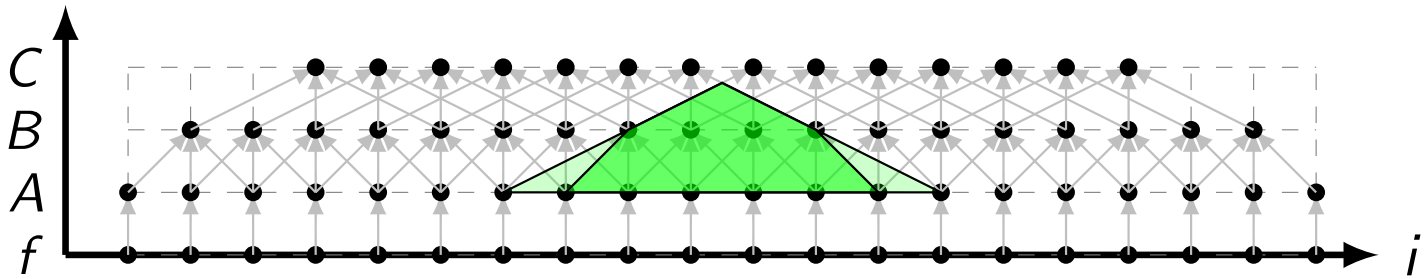

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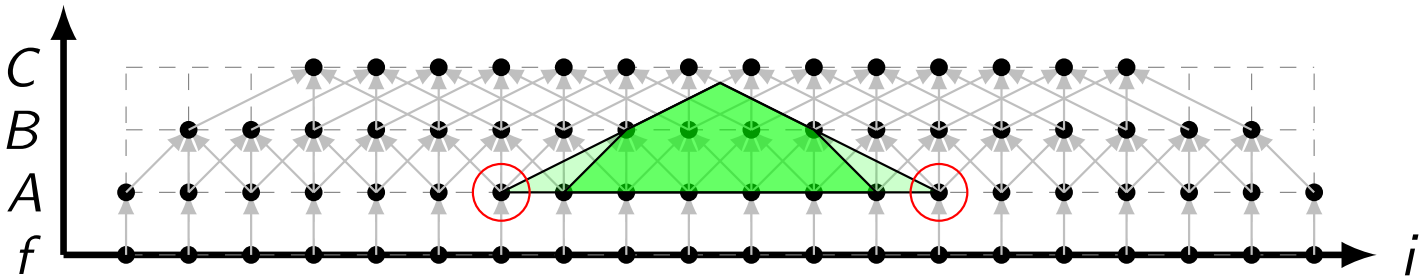

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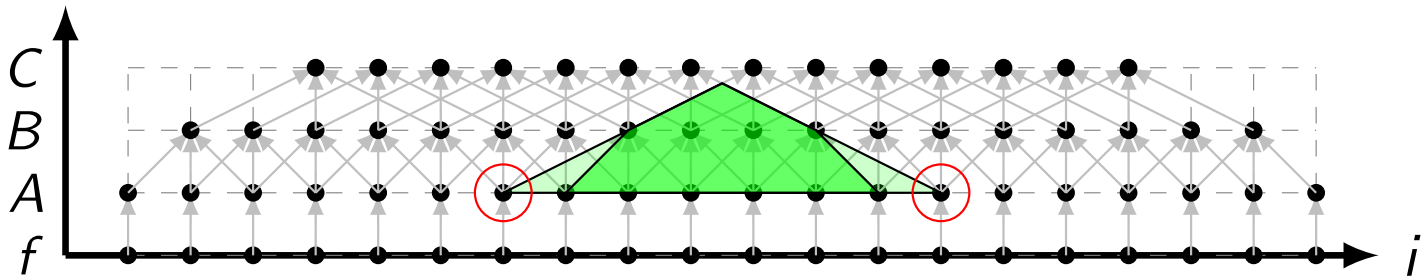


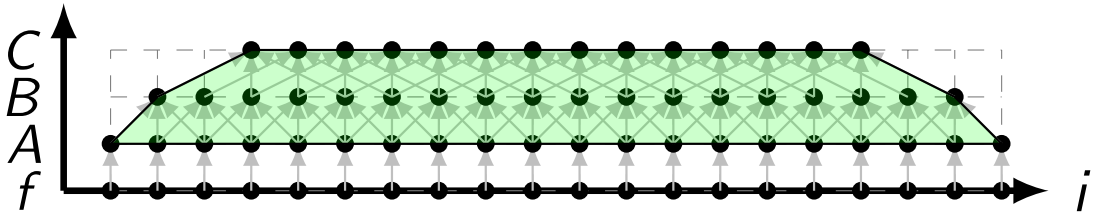
Overlapped tiling on the iteration space

We mitigate redundant computation by shrinking the shadows; better performance than a rescheduling-based technique.

Comparing with PolyMage

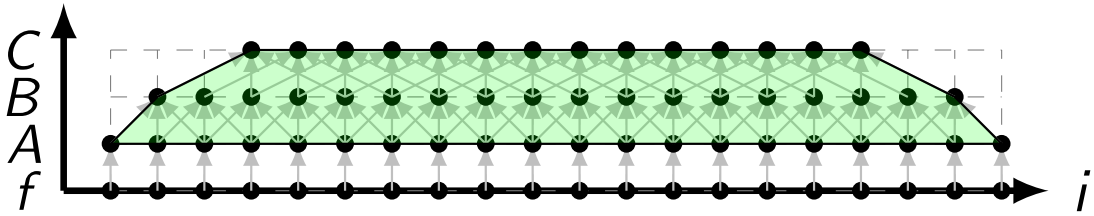
	PolyMage	Our work
Redundancy	More	Less
Implementation	With shifting	With/Without shifting
Applicability	Domain-specific language	General-purpose language
Targets	CPU	CPU & GPU

Overlapped Tiling With Shifting



Iteration Space

Overlapped Tiling With Shifting



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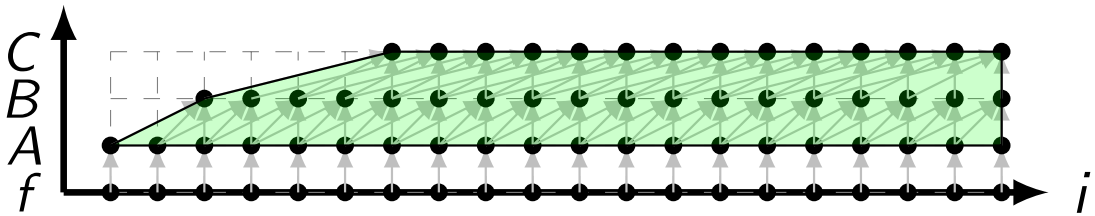

Overlapped tiling with shifting

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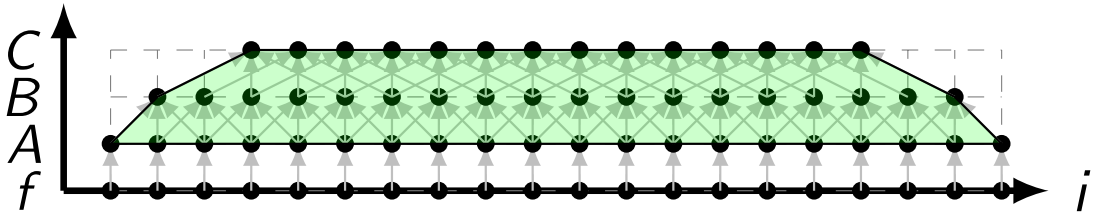

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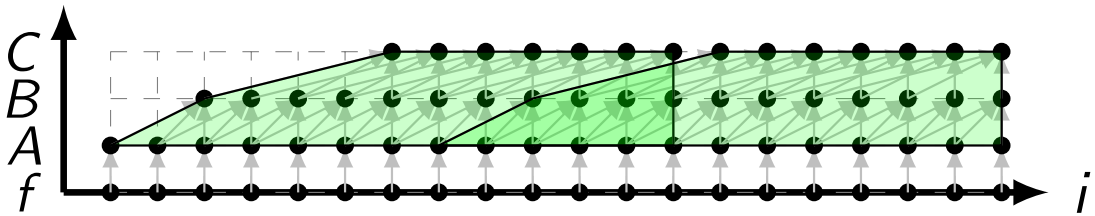

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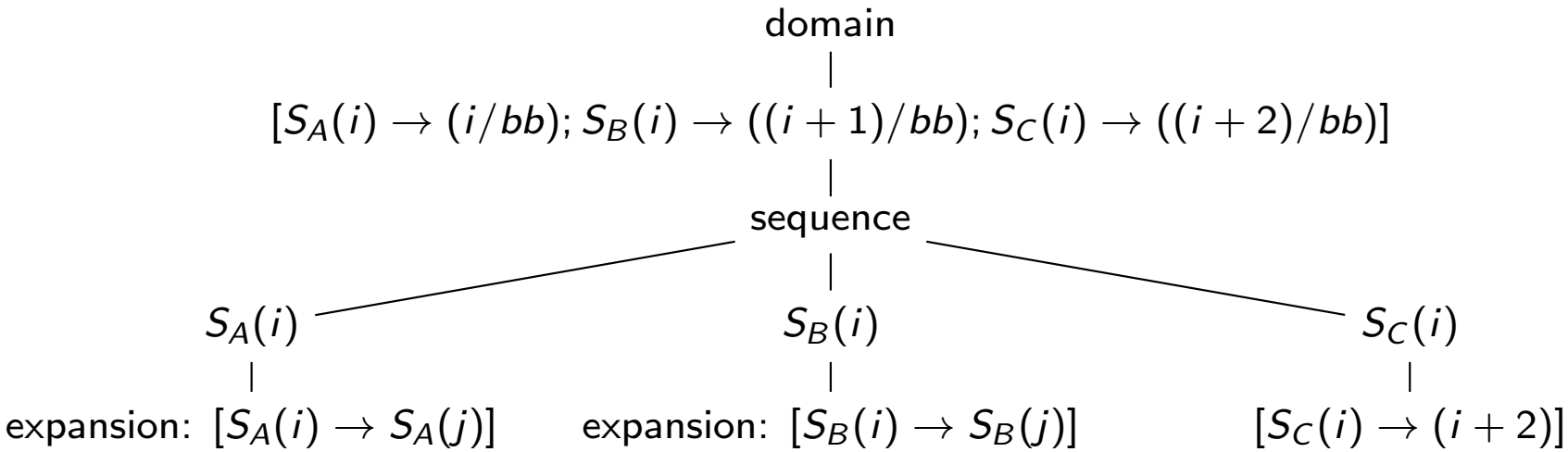
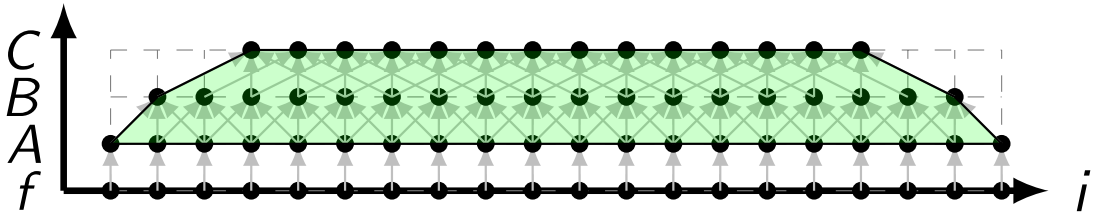


Schedule tree

Overlapped Tiling With Shifting



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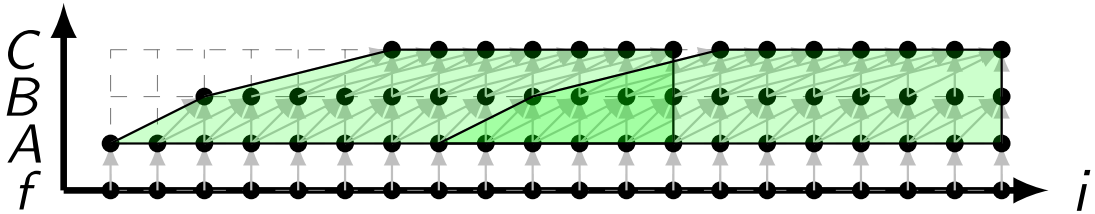

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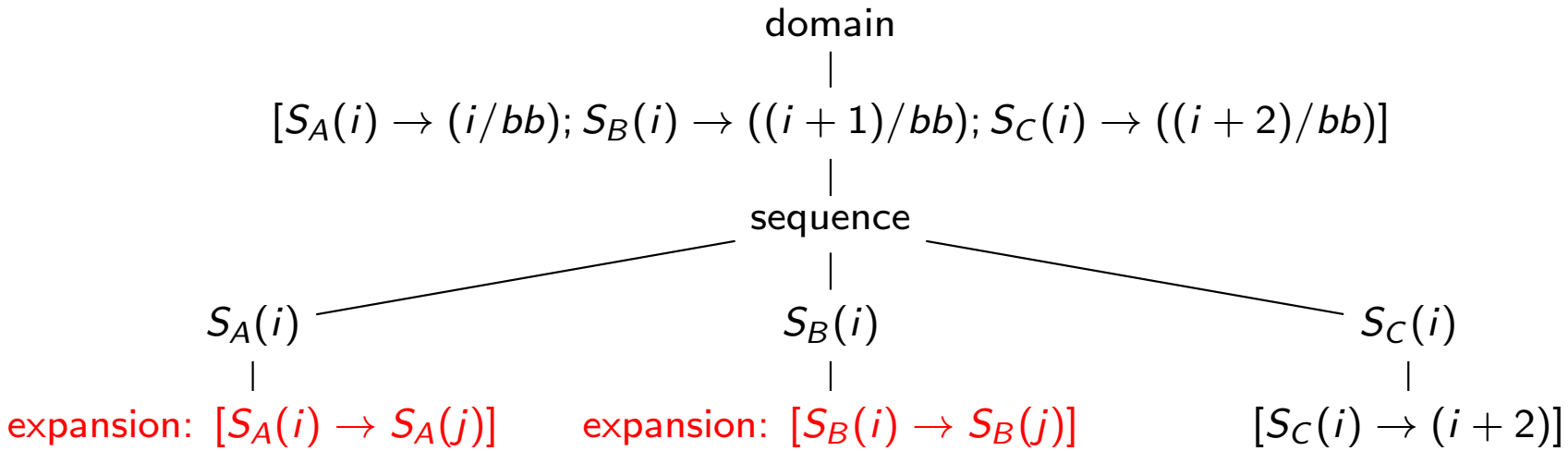

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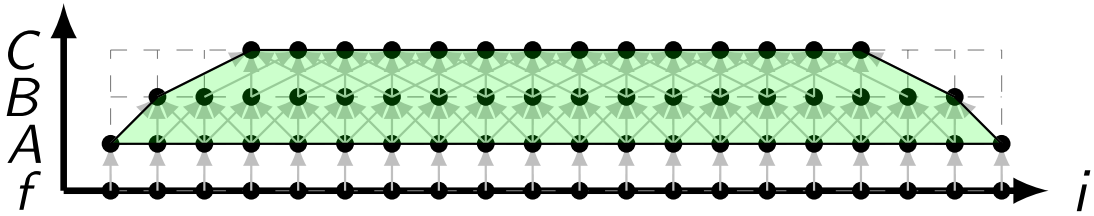
Overlapped Tiling Without Shifting



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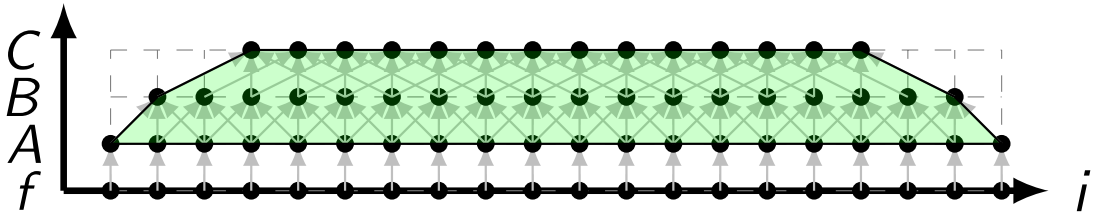

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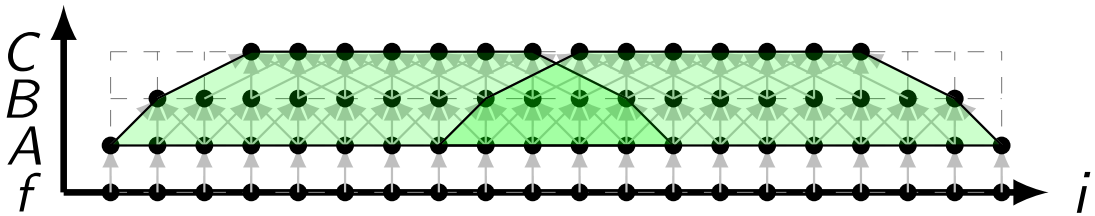

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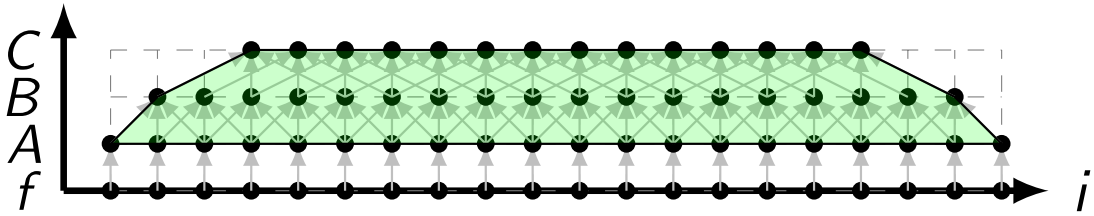

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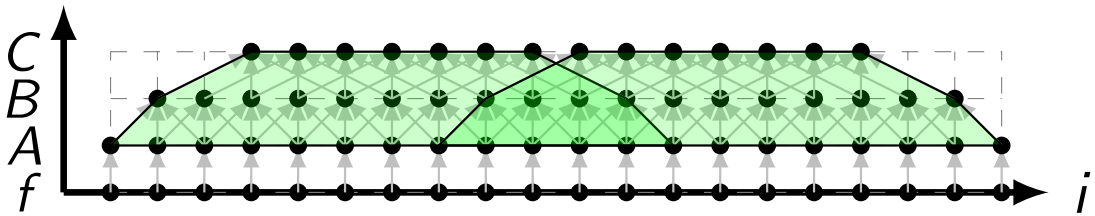

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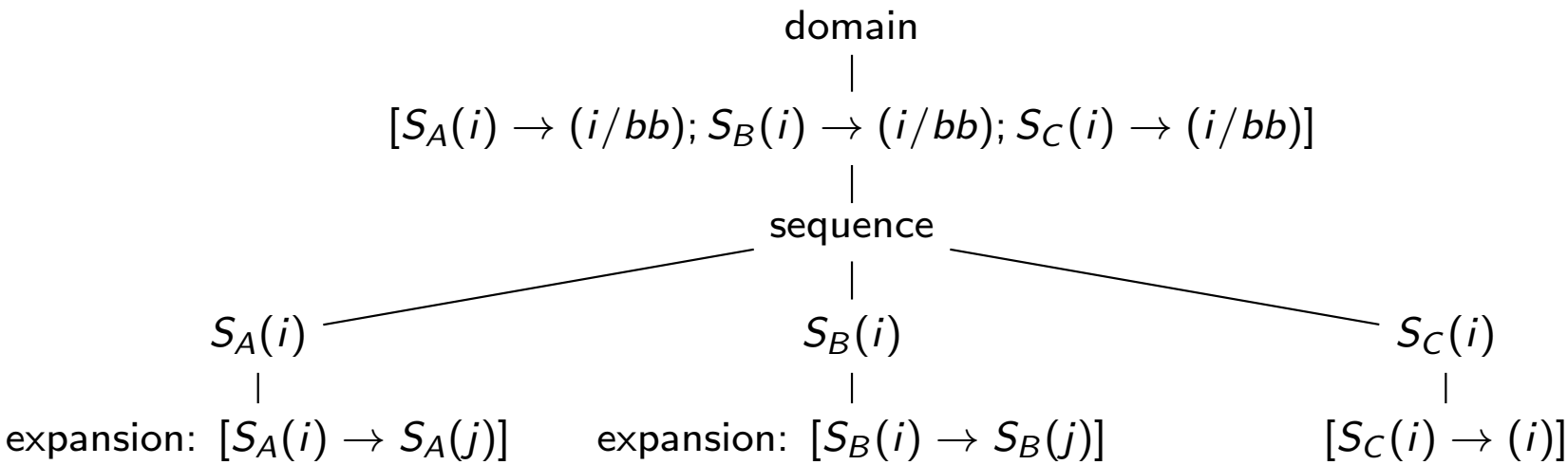

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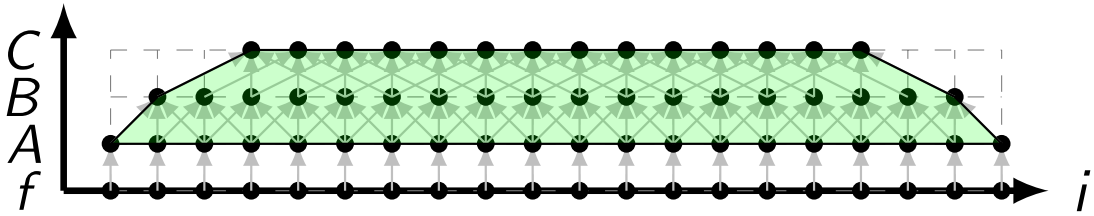

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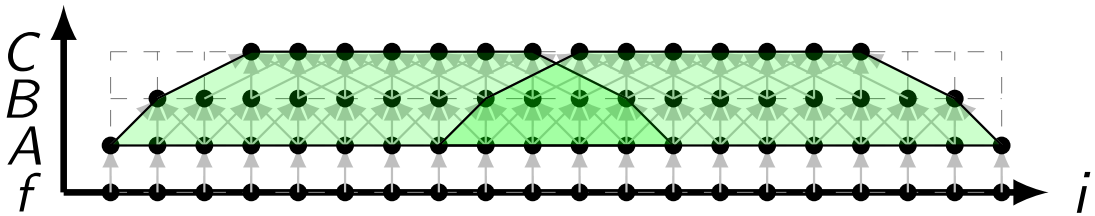

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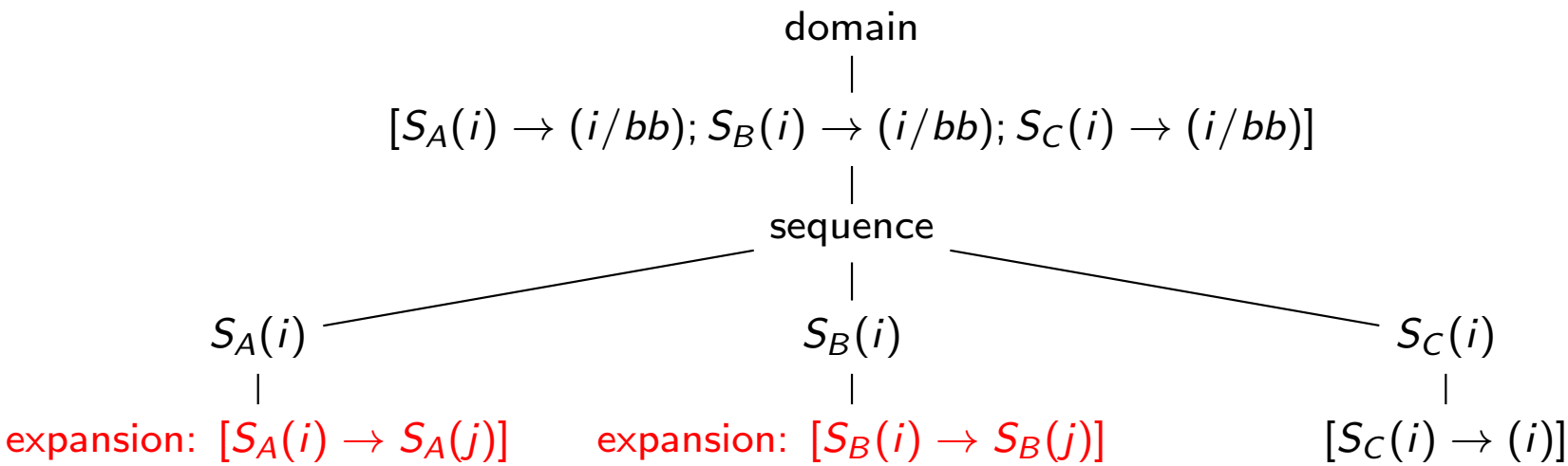
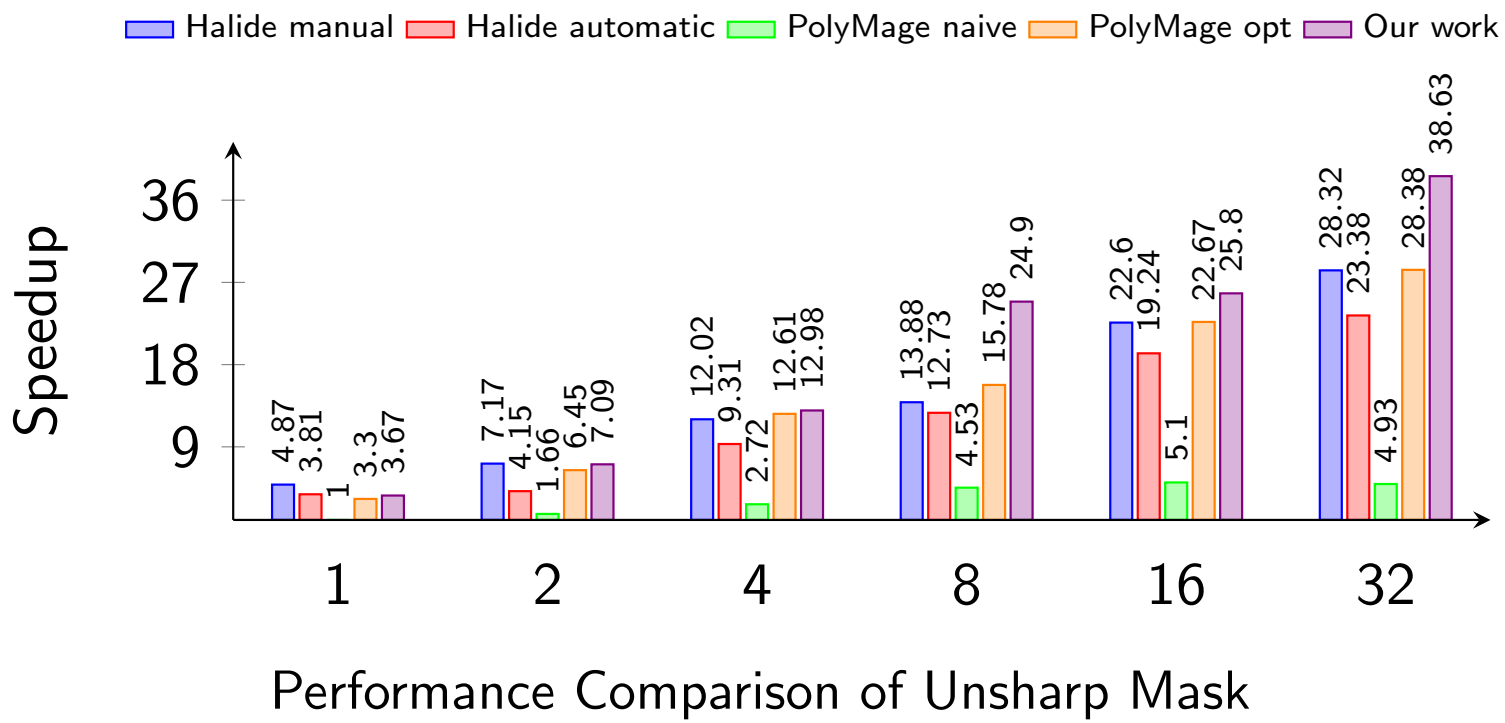


Schedule Tree

Experimental Setup and Methodology

- Code generator: PPCG (version `ppcg-0.07-26-g236d559`).
- Architecture:
  - CPU: 32-core Intel Xeon(R) E5-2683 v4 @2.10GHz
  - GPU: NVIDIA Quadro K4000
- Compilation:
  - CPU: ICC`18.0` (*-O3 -xHost -qopenmp -ipo*)
  - GPU: NVCC`9.0` (*-O3*)
- Baseline:
  - sequential PolyMage naive code (without tiling) [MVB15]
  - CUDA code generated by PPCG (parallelogram tiling) [VCJC+13]
- Comparison:
  - Halide manual and automatic scheduling [RKBA+13], PolyMage naive and optimized scheduling [MVB15]

Performance Comparison on CPU



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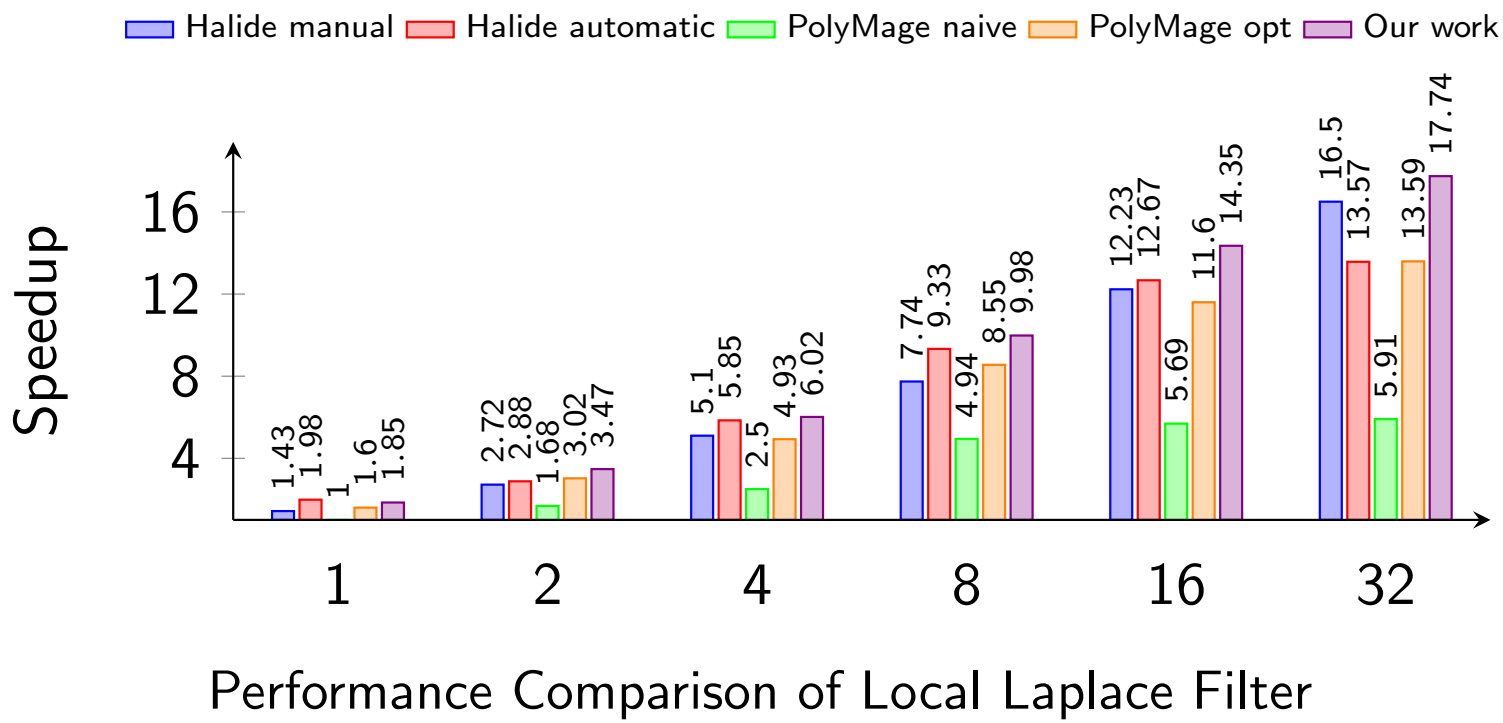
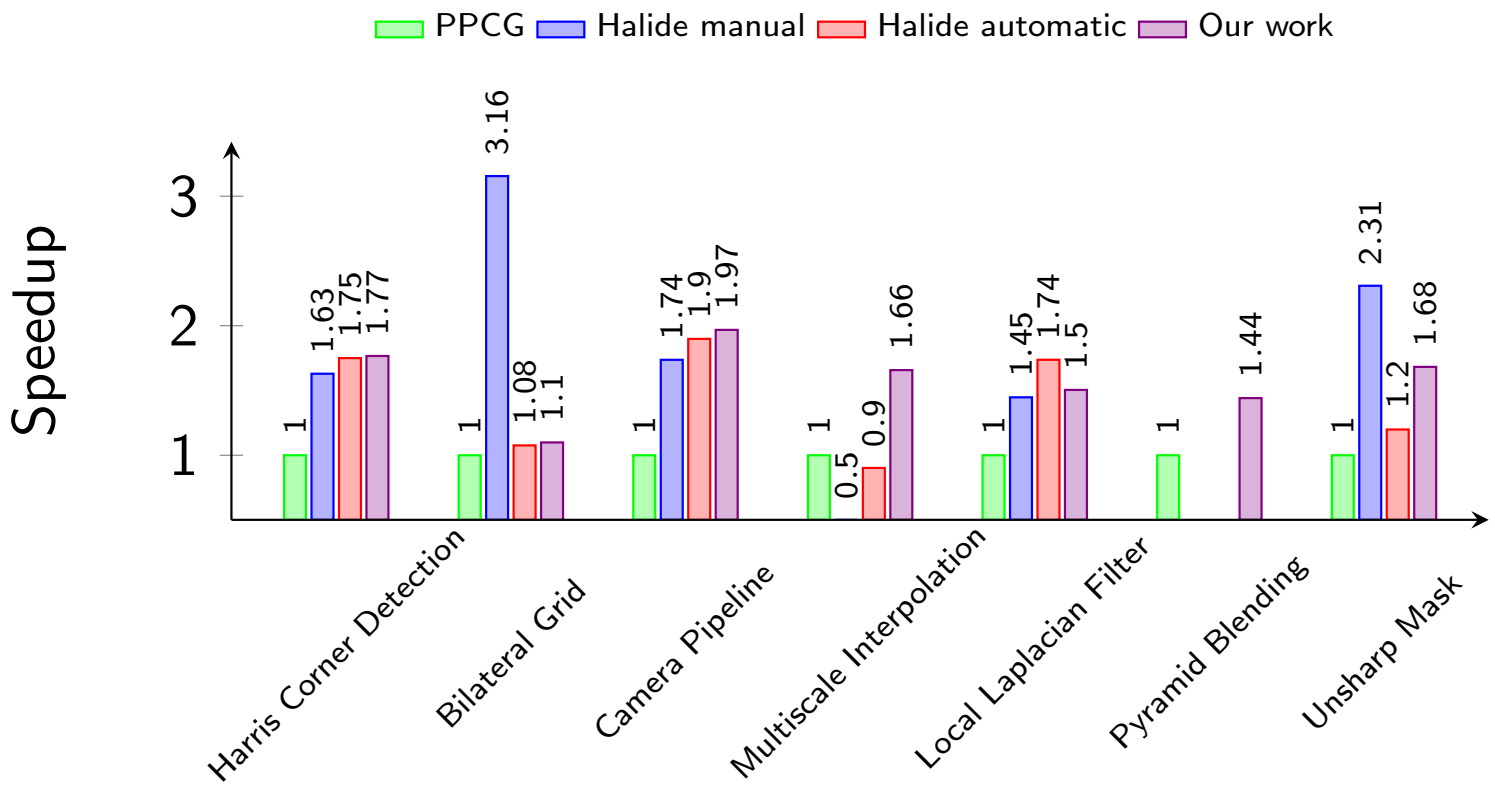


Please refer to our poster for more experimental data on the remaining benchmarks, with a detailed comparison with the state of the art.

Performance Comparison on GPU



Performance Comparison of All Benchmarks on GPU

Our technique is also applicable to iterated stencils. Please check on our poster for the evaluation on both CPU and GPU.

Conclusion and Future Work

- We implemented a general purpose overlapped tiling technique in a polyhedral framework.
- We implemented overlapped tiling technique with/without shifting.
- Our work can generate codes for both CPU and GPU.
- We get better performance due to less redundant computation.
- Future work: finish the experiments and prepare the paper submisson.

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