

A Brief History of Synchronous Programming

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A French researcher go to a conference...



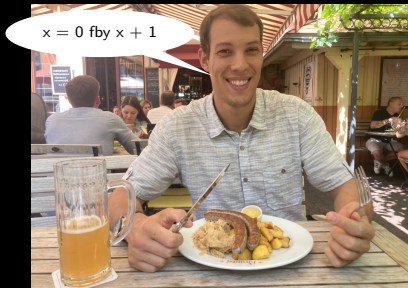




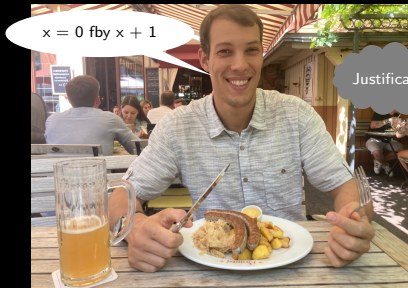












Justificatifs!



How to **specify, program, verify** the software of this small printer?

What is different from other programs?

Physical components, e.g., **sensors, actuators**, stepper motor (paper roll), etc.

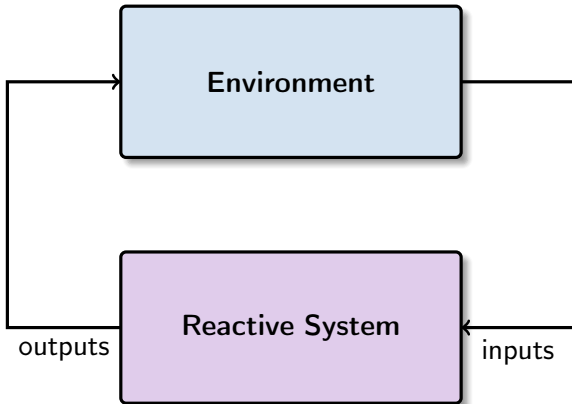
Control permanently (temperature), fast enough, regularly (the motor), etc.

More widely...

fly-by-wire command of a plane, on-board control of a train, the management of energy in a car, etc.

They are all **embedded reactive systems**.

What is it all about?



Write Assembly/C/C++/JavaScript/Python/OCaml/Coq by hand?

And compare it to what?

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What is the specification?

And if we have a formal specification,

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in what programming language to write it?

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there is no run-time error;

the memory used is bounded and known statically;

the worst-case execution time is bounded and known statically;

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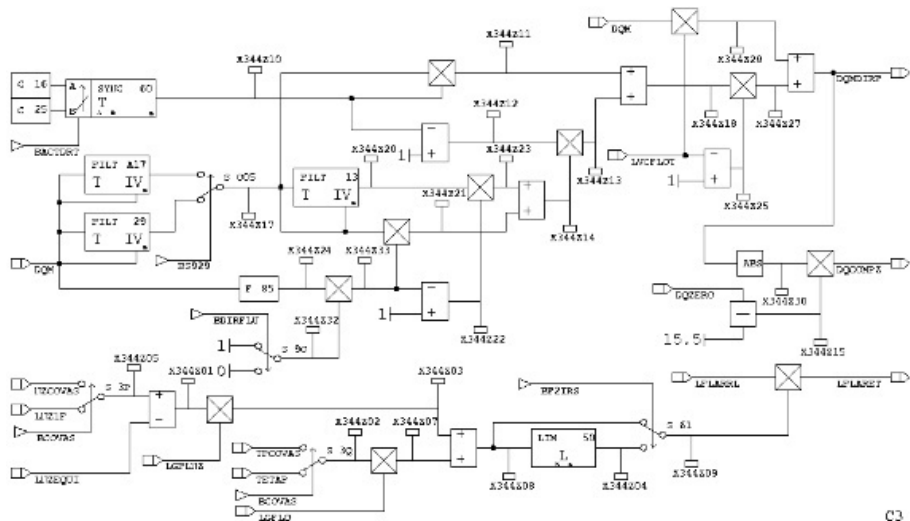
the memory used is bounded and known statically;

the worst-case execution time is bounded and known statically;

the executed code faithfully implements the specification.

A language for writing executable math specifications?

SAO (Spécification Assistée par Ordinateur) — Airbus 80's



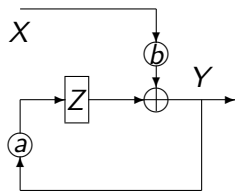
Accurate drawings

Engineers in control/signal processing had precise maths before the use of computers.

Sampled systems: stream equations, state machines, etc.

Example: a linear filter

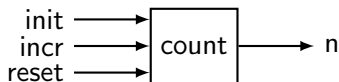
$$Y_0 = bX_0, \forall n Y_{n+1} = aY_n + bX_{n+1}$$



...but not executable! Write code and convince that it is correct.

How to make those maths executable?

Somewhere in Grenoble... the language Lustre (1987) [CHPP87]



```
node COUNT (init, incr: int; reset: bool)
  returns (n: int);
let
  n = init ->
    if reset then init else pre(n) + incr;
tel;
```

Programming with stream equations

A discrete system: a **function of sequences**; the sequences are **synchronous**.

X	1	2	1	4	5	6	...
Y	2	4	2	1	1	2	...
$X + Y$	3	6	3	5	6	8	...
$pre\ X$	<i>nil</i>	1	2	1	4	5	...
$Y \rightarrow X$	2	2	1	4	5	6	...

Equation $Z = 0 \rightarrow pre\ Z + X + Y$ means $Z_0 = 0 \wedge Z_n = Z_{n-1} + X_n * Y_n$.

Time is **logical**: inputs X and Y arrive "**at the same time**"; the output Z is produced "**at the same time**"

Euh... is-it real-time?

Reason in **worst case**: check that the generated code produces the output before the next input arrives.

The beautiful idea of Lustre

A synchronous interpretation of the **Kahn and MacQueen networks** [Kah74, KM77] and **Lucid** [AW85].

Express directly sampled models from control engineering.

Analyze/transform/simulate/test/verify them.

Automatically translate them into executable code.

A Lustre program is a **precise specification**.

An immediate resonance with industrial practice:

- SAO (Spécification Assistée par Ordinateur) - Airbus.
- Saga - Merlin Gerin

SCADE: Safety Critical Application Dev. Env. (Verilog, 95)

The screenshot displays the SCADE IDE interface for a project named 'libdigital.vsp'. The main workspace shows a Verilog circuit diagram for a rising edge trigger. The circuit includes a counter block labeled 'count_down' with a 'NumberOfCycle' input. The output of the counter is connected to an AND gate, which also receives a 'false' input. The output of this AND gate is connected to an OR gate, which also receives a 'false' input. The output of the OR gate is connected to an AND gate, which also receives a 'false' input. The output of this final AND gate is connected to the 'RER_Output' signal. The circuit also includes a 'PRE' block, a 'NumberOfCycle' input, and a 'false' input. The interface shows a project tree on the left with various blocks like 'Constant Blocks', 'Variable Blocks', 'Type Blocks', 'Operators', 'count_down', 'EtherEdge', 'FallingEdge', 'FallingEdgeNoRetrigger', 'FallingEdgeRetrigger', 'FlipFlopK', 'FlipFlopReset', 'FlipFlopSet', 'RisingEdge', 'RisingEdgeNoRetrigger', 'RisingEdgeRetrigger', 'Interface', 'eq_risingEdgeRetrigger', and 'Toggle'. The bottom window shows a message log with the following text: 'Loading project libdigital.vsp', 'Constant values updated to new format', and 'Successfully loaded project libdigital.vsp'. The status bar at the bottom indicates 'Messages | Dump | Build | Simulator'.

At the same time...

In Rennes: the Signal language (1987) [BLJ91]

Same influence and approach as Lustre but much more expressive.

A system: a **relation between sequences**.

Write specifications (partial, non-deterministic) of a system.

A Signal program is used to specify the interface of a component.

Study refinement relations.

Sildex industrial tool: based on Signal (TNI-Software then DS).

À Nice: the Esterel language (1984) [Gon88, BG92]

“Control” dominated systems (e.g., Mealy machines) and their transcription into sequential circuits.

Theoretical computer science (process calculus, lambda calculus, semantics).

Several radical ideas:

- A programming style closer to computer science: sequence, loops, interrupt, suspension of task, parallel composition, hierarchy, etc. to increase expressiveness.
- Several semantics, in SOS form.
- How to make this portable and deterministic?

Composition of boolean automata (e.g., Argos) [Mar92]

The beautiful idea of Esterel

Do as if the machine were computing infinitely fast!

Reconcile parallelism (for expressiveness) and determinism (for safety) ².

A new discovery: compile Esterel into circuits (Lustre).

```
module ABRO
input A, B, R;
output C
loop
  [await A || await B];
  emit C
each R;
end module
```

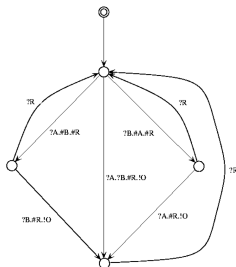


Figure 3.1: The ABRO Mealy machine

Industrial tool: Esterel-Studio then start-up Esterel-Technologies (1999).

²“Write things once” (The Esterel Language Primer Version 5.91, G. Berry, 2000).

The same synchronous approach

With very different programming styles, all these languages share the same principles

- (1) reason ideally;
- (2) Compile the parallelism and compute the WCET of the generated code.

It's much easier.

Some programs are monsters...

how to reject them?

Different time scales

Synchronize slow and fast processes?

<i>X</i>	1	2	3	4	5	...
<i>half</i>	<i>true</i>	<i>false</i>	<i>true</i>	<i>false</i>	<i>true</i>	...
<i>X when half</i>	1		3		5	...
<i>X + (X when half)</i>	2		5		8	...

```
let half = true -> not (pre half);  
  o = x + (x when half);  
tel
```

Define the sequence: $\forall n \in \mathbb{N}. o_n = x_n + x_{2n}$

- cannot be implemented with bounded memory (buffer);
- reject it statically: we can do it by **typing** [CP96, CP03].

Analyze dependences between signals

Programs have zero solutions (*deadlock*) or too many (*non-determinism*)

In Lustre/Signal

- $x = y + 1$ and $y = x + 2$
- $y = x$ and $x = y$

For Lustre, a simple choice: “**Syntactic causality**” [CHPP87]:

“every loop must cross a delay”, i.e., partial order between calculations.

This analysis can be done in a modular way, by **typing** and independent of clock calculus [CP01, BBC⁺14]. And we can compile in independent blocks [PR09].

For Signal, conditional dependencies: “ x depends on y if c ”.

Detect “true” cycles. Combines the computation of clocks and causality; analysis and code generation are more complex [ABG95].

Analyze dependences between signals

In Esterel

- `present S else emit S`
- `present S1 then emit S2 || present S2 then emit S1`
- `present I then
 present O2 then emit O1 else present O1 then emit O2`

Two discoveries [Draft book'02] ³

Constructive semantics by calculating a fixed-point at each instant [Gon88, Ber02].

Are there any undetermined signals?

For Esterel, the “good” notion of causality is that of the **électricité**.

“If we wire the synchronous program, are the outputs stable?”

Coincides with what is provable in **constructive logic** [MSB12]

³The Constructive Semantics of Pure Esterel Draft Version 3, 2002, G. Berry.

A bit later, somewhere between Grenoble and Jussieu...

Lucid Sychrone and ReactiveML

An idea of Paul Caspi, in 1994, in Grenoble.

“Marc, take a good look, we can write recursive Lustre programs in a few lines of LazyML!”

Very expressive: higher order, type inference, recursion, etc.

but the “monsters” are still there.

typing, typing, typing... and adapt the compilation.

Lucid Sychrone (95-06) [CP96, Pou06]

Build a functional synchronous language with ML features.

ReactiveML (05-15) [MP05]

Synchronous parallelism in an ML-like language (OCaml)

Boussinot model [Bou91]: delayed reaction to absence.

Functional and synchronous: quesaco? ⁴

Operations on streams in a language *a la ML*.

A synchronous interpretation [CP96, CP98] of Kahn & MacQueen's networks.

Make it a **laboratory** to experiment with new ideas.

New programming constructs: pattern matching, signals, last, automata, higher-order, etc.

Express the static semantics in term of dedicated type systems: clock calculus [CP96, CP03], causality analysis [CP01, BBC⁺14], initialization analysis [CP04], etc.

A semantics by translation/collapse: being able to explain the high-level constructions in terms of **clocked data-flow equations with reset**.

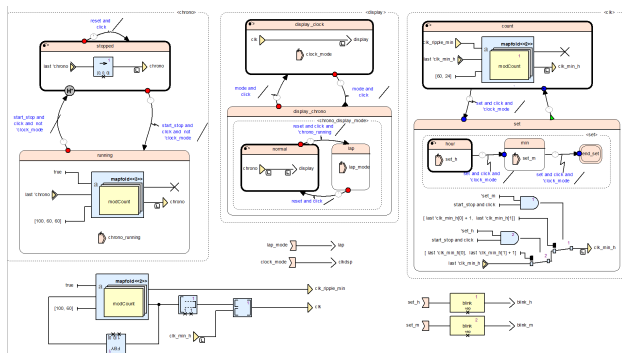
To ensure that the proposed new constructs are **conservative**.

A collaboration with Jean-Louis Colaço (Esterel-Tech./ANSYS).

⁴What is this?

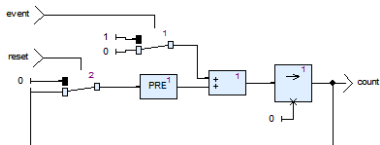
Scade/KCG 6 [CPP17]

- A new language and compiler, in 2008; written in OCaml;
- many ideas from Lucid Sychrone.



Are your drawings correct? Prove it!

'What you prove is what you execute' (Berry '89)



```
L1 = pre L7;  
L2 = (L11) -> (L5);  
L3 = event;  
L4 = reset;  
count = L2;  
L5 = L6 + L1;  
L6 = if L3 then (L8) else (L9);  
L7 = if L4 then (L10) else (L2);  
L8 = 1;  
L9 = 0;  
L10 = 0;  
L11 = 0;
```

code gen.

```
void counter_reset(outC_counter *outC)  
{  
    outC->init = kcg_true;  
}  
  
void counter(inC_counter *inC, outC_counter *outC)  
{  
    kcg_int tmp;  
  
    if (outC->init) {  
        outC->count = 0;  
    }  
    else {  
        if (inC->event) {  
            tmp = 1;  
        }  
        else {  
            tmp = 0;  
        }  
        outC->count = tmp + outC->_L9;  
    }  
    if (inC->reset) {  
        outC->_L9 = 0;  
    }  
    else {  
        outC->_L9 = outC->count;  
    }  
    outC->init = kcg_false;  
}
```

A certified compiler? an idea born in 1992/1993

Scade: a language from Lustre (common lab VERILOG/IMAG = VERIMAG).

Make a **certified compiler** for the strictest **standards** avionics.

Avoid having to **recheck** that the generated code is correct with respect to the source.

Based on the simple and precise definition of Lustre and its code generation.

The major evolutions of the language (Scade 6) and of the compiler were all guided by this objective.

An **obligation of means** vs an **obligation of result** (e.g., CompCert).

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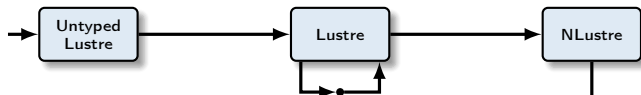
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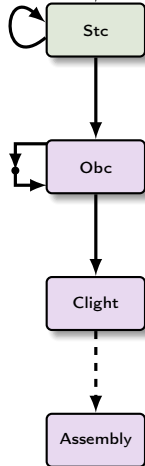
An **obligation of means** vs an **bligation of result** (e.g., CompCert).

Can (and how) be developed a proven synchronous compiler?

Vélus: a proven Lustre compiler to CompCert

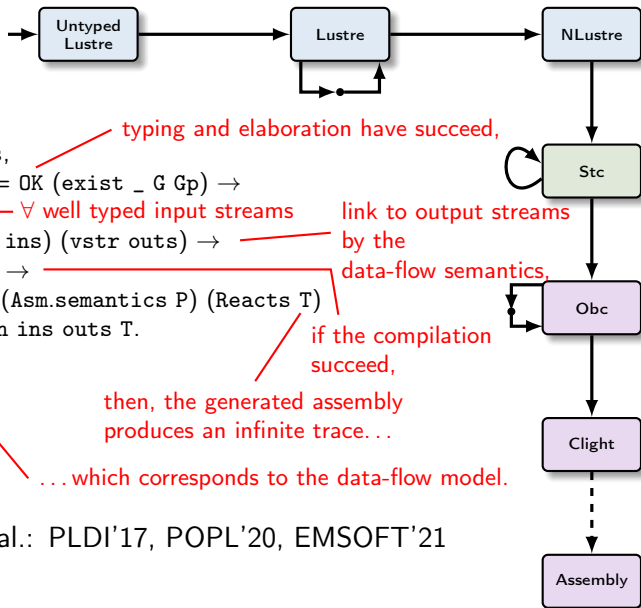


Theorem `behavior_asm`:

$$\begin{aligned} &\forall D \ G \ Gp \ P \ \text{main} \ \text{ins} \ \text{outs}, \\ &\text{elab_declarations } D = \text{OK} \ (\text{exist } _ \ G \ Gp) \rightarrow \\ &\text{wt_ins } G \ \text{main} \ \text{ins} \rightarrow \\ &\text{sem_node } G \ \text{main} \ (\text{vstr } \text{ins}) \ (\text{vstr } \text{outs}) \rightarrow \\ &\text{compile } D \ \text{main} = \text{OK} \ P \rightarrow \\ &\exists T, \ \text{program_behaves} \ (\text{Asm.semantics } P) \ (\text{Reacts } T) \\ &\quad \wedge \ \text{bisim_io } G \ \text{main} \ \text{ins} \ \text{outs} \ T. \end{aligned}$$


- Timothy Bourke et al.: PLDI'17, POPL'20, EMSOFT'21
- 100kLOC de Coq.
- <https://velus.inria.fr>

Vélus: a proven Lustre compiler to CompCert



Theorem `behavior_asm`:

$\forall D G Gp P \text{ main ins outs,}$

`elab_declarations D = OK (exist _ G Gp) \rightarrow`

`wt_ins G main ins \rightarrow $\neg \forall$ well typed input streams`

`sem_node G main (vstr ins) (vstr outs) \rightarrow`

`compile D main = OK P \rightarrow`

$\exists T, \text{program_behaves (Asm.semantics P) (Reacts T)}$

$\wedge \text{bisim_io G main ins outs T.}$

typing and elaboration have succeed,

link to output streams by the data-flow semantics,

if the compilation succeed,

then, the generated assembly produces an infinite trace...

... which corresponds to the data-flow model.

- Timothy Bourke et al.: PLDI'17, POPL'20, EMSOFT'21
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The stepper motor?

<https://vertmo.org/jsofocaml/try-velus/>⁵

⁵Thanks to Timothy Bourke and Basile Pesin.

A short focus on Causality

It has been the subject of strong debates.

There is no absolute notion of causality: there is not one that is better than the other.

Some are more powerful (they accept more program).

The choice is **determined by the code you target**, e.g., circuit or software.

For circuits, if cyclic circuits are forbidden by the synthesis tool, why fighting for constructive causality?

For software, different compromises, e.g., code size of the target code.

A demo with Zrun

An experiment with the zrun interpreter of Zélus ⁶

<https://github.com/INRIA/zelus/tree/work>

The causality in Lustre vs Signal vs Esterel correspond to different interpretations of the conditional. With zrun, you can try several.

Syntactic Causality (Lustre)

<i>*if \perp then _ else _</i>	$\stackrel{def}{=}$	\perp
<i>*if _ then \perp else _</i>	$\stackrel{def}{=}$	\perp
<i>*if _ then _ else \perp</i>	$\stackrel{def}{=}$	\perp
<i>*if true then x else _</i>	$\stackrel{def}{=}$	x
<i>*if false then _ else y</i>	$\stackrel{def}{=}$	y

⁶See previous talks at SYNCHRON - winter 2019 and 2021.

Causality

Lazy Causality

**if \perp then _ else _* $\stackrel{def}{=} \perp$

**if true then x else _* $\stackrel{def}{=} x$

**if false then _ else y* $\stackrel{def}{=} y$

Constructive Causality (Esterel)

**if \perp then v_1 else v_2* $\stackrel{def}{=} \text{if } v_1 = v_2 \text{ then } v_1 \text{ else } \perp$

**if true then x else _* $\stackrel{def}{=} x$

**if false then _ else y* $\stackrel{def}{=} y$

Causality

With the following definition for the or/and gates:

$$*or(x, y) \stackrel{def}{=} \text{if } x \text{ then true else } y$$

$$*and(x, y) \stackrel{def}{=} \text{if } x \text{ then } y \text{ else false}$$

With the first interpretation, the two operators are strict. With the second one, they are “sequential” (left-to-right); with the third one, it coincides with the 3-valued logic for boolean operators.

$$*or(true, _) = true$$

$$*or(_, true) = true$$

$$*or(false, x) = x$$

$$*or(x, false) = x$$

$$*and(false, _) = false$$

$$*and(_, false) = false$$

$$*and(true, x) = x$$

$$*and(x, true) = x$$

Examples in Zélus

Examples available at:

<https://github.com/INRIA/zelus/tree/work/zrun/tests/good/>.

A simple counter.

The cyclic circuit of Malik.

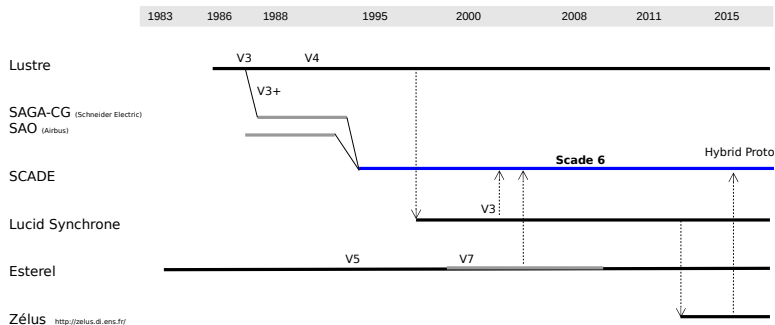
The Bus arbiter by R. de Simone.

A surprise: this later example does not need the interpretation given by Esterel for the *or* and *and* gate. It is enough to use a lazy conditional. See `arbiter.zls`.

Modular causality analysis

The causality analysis in Zélus and Scade is done modularily through a **dedicated type system**. In the academic Lustre compiler, it is done on the result of the static inlining of nodes.

Timeline



I forgot very important subjects and works.

Synchronous observers [HLR92, HLR93]

A synchronous program that observes the inputs/outputs.

A wide set of formal verification techniques, actively participating in the progress of model-checking.

Direct links with circuit verification.

e.g., enumerative methods (before 90); symbolic by BDD (90-00); based on SAT (00-08); SMT (08-).

Academic tools (e.g., Lesar, Kind, Kind2 [CMST16]) and industrial.

The idea of synchronous observers has been taken up everywhere, e.g., Scade, Simulink.

Original synchronous languages for specifying properties: HLL (RATP and Prover) [OBC18], Lutin [RRJ08], Stimulus, CCSL [ZWCM21], etc.

An abundance of languages and compilers

Many languages/compilers to test/experiment with new ideas.

Integrate ideas from the synchronous into an existing language.

ReactiveC (from reactive in C), SugarCubes (from reactive in Java), ReactiveML (from reactive in ML), HipHop (from reactive to Esterel in JavaScript), etc.

To express finer (C-style) imperative features in a synchronous language, e.g. SCCharts [vHDM⁺14].

To express and exploit periodic calculations: Lucy-n [MPP10], Prelude [CBF⁺11].

And many others... SaxoRt compiler from Esterel, Quartz language, Shim, Blech, etc.

Distribute code, quasi-synchronous model, generation into tasks, etc.

The SYNCHRON workshop

An annual and uninterrupted workshop since 1994.

<http://synchron2021.inria.fr>



A precious and unique place to present on-going or more complete work.

Invite colleagues on new topics, e.g., synchronous programming for music, modeling of hybrid systems.

No publication, no selection committee, no referee, no program.

but open debates, confrontation of ideas.

Conclusion

- Dedicated, parallel and deterministic languages;
- adapted to the mathematical culture and the practice of engineers;
- adopted from the beginning.
- Do not compromise on principles: static and dynamic semantics specified in detail as well as the compiler.
- A continuous evolution of languages, compilation methods, compile-time checks.
- Ideas used in other applications: web, high frequency trading, mixed music, ChatBot, etc.
- A direct impact on industrial tools used every day.
- Some to build software; others to specify/verify properties of systems implemented otherwise.

And the story continues

- Industrial certification: can Coq specs complement/replace current (human) verification steps?
- Compilation that includes **translation validation**, independent testing that uses an **executable semantics**.
- Relax some synchronism constraints but control **end-to-end latencies** (Airbus's practice, etc.).
- Express **real-time constraints** and exploit them to generate sequential code, in **tasks** or **parallel**.
- Write hybrid models; probabilistic.
- An old topic: calculating with arrays. What's new?
A surprise: the principles and style of the language SISAL⁷ works well with Lustre.

⁷Stream and Iteration in a Single Assignment Language [FCO90]

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