A Characterization of Box $\frac{1}{d}$-integral Binary Clutters

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Abstract. Let Q_6 denote the port of the dual Fano matroid F_7^* and let Q_7 denote the clutter consisting of the circuits of the Fano matroid F_7 that contain a given element. Let $\mathcal{L}$ be a binary clutter on E and let $d \geq 2$ be an integer. We prove that all the vertices of the polytope $\{x \in \mathbb{R}^E : x(C) \geq 1 \text{ for } C \in \mathcal{L}\} \cap \{x : a \leq x \leq b\}$ are $\frac{1}{d}$-integral, for any $\frac{1}{d}$-integral a, b, if and only if $\mathcal{L}$ does not have Q_6 or Q_7 as a minor. Applications to graphs are presented, extending a result from [7].

1 The main result

Let $\mathcal{L}$ be a collection of subsets of a set E. $\mathcal{L}$ is called a *clutter* if, for all $A, B \in \mathcal{L}$, $A = B$ whenever $A \subseteq B$. Given an integer $d \geq 1$ and a vector x, x is said to be $\frac{1}{d}$-*integral* if dx is integral, i.e. all the components of x belong to $\frac{1}{d}\mathbb{Z} := \{\frac{i}{d} : i \in \mathbb{Z}\}$.

Definition 1.1 *Let $\mathcal{L}$ be a clutter on E. We say that $\mathcal{L}$ is* box $\frac{1}{d}$-integral *if $\mathcal{L} = \{\emptyset\}$ or, for all $a, b \in (\frac{1}{d}\mathbb{Z})^E$, each vertex of the polyhedron*

$$Q(\mathcal{L}, a, b) := \{x \in \mathbb{R}_+^E : x(C) \geq 1 \textit{ for } C \in \mathcal{L},\ a_e \leq x_e \leq b_e \textit{ for } e \in E\}$$

is $\frac{1}{d}$-integral. Equivalently, $\mathcal{L}$ is box $\frac{1}{d}$-integral if, for all subsets $I \subseteq E$ and all $a \in (\frac{1}{d}\mathbb{Z})^I$, each vertex of the polyhedron

$$Q(\mathcal{L}, a) := \{x \in \mathbb{R}_+^E : x(C) \geq 1 \textit{ for } C \in \mathcal{L},\ x_e = a_e \textit{ for } e \in I\}$$

is $\frac{1}{d}$-integral.

We shall mostly use the second definition for box $\frac{1}{d}$-integral clutters.

Given a clutter $\mathcal{L}$ on E and a subset Z of E, set $\mathcal{L}\backslash Z = \{A \in \mathcal{L} : A \cap Z = \emptyset\}$ and let $\mathcal{L}/Z$ consist of the minimal members of $\{A - Z : A \in \mathcal{L}\}$; both $\mathcal{L}\backslash Z$ and $\mathcal{L}/Z$ are clutters. The operations are called, respectively, *deletion* and *contraction* of Z. A *minor* of $\mathcal{L}$ is obtained from $\mathcal{L}$ by a sequence of deletions and contractions.

Let $\mathcal{M}$ be a matroid on a groundset $E \cup \{\ell\}$, where ℓ is a distinguished element of the groundset, and let $\mathcal{C}$ denote the family of circuits of $\mathcal{M}$. The family $\{C : C \cup \{l\} \in \mathcal{C}\}$ is a clutter, called the *ℓ-port* of $\mathcal{M}$. A clutter is said to be *binary* if it is the port of some binary matroid.

The binary clutters Q_6 and Q_7 are defined, respectively, on six and seven elements. Q_6 is the clutter on the set $\{1,2,3,4,5,6\}$ consisting of the sets $\{1,3,5\}$, $\{1,2,6\}$, $\{2,3,4\}$ and $\{4,5,6\}$. Q_7 is the clutter on the set $\{1,2,3,4,5,6,7\}$ consisting of the sets $\{1,4,7\}$, $\{2,5,7\}$, $\{3,6,7\}$, $\{1,2,6,7\}$, $\{1,3,5,7\}$, $\{2,3,4,7\}$ and $\{4,5,6,7\}$.

The following result is the main result of the paper. Applications to graphs are given in Section 5.

THEOREM 1.2 *Let $\mathcal{L}$ be a binary clutter on a set E, $\mathcal{L} \neq \{\emptyset\}$. The following assertions are equivalent:*
(i) $\mathcal{L}$ does not contain Q_6 or Q_7 as a minor,
(ii) $\mathcal{L}$ is box $\frac{1}{d}$-integral for each integer $d \geq 1$,
(iii) $\mathcal{L}$ is box $\frac{1}{d}$-integral for some integer $d \geq 2$.

Observe that, for $d = 1$, $\mathcal{L}$ is box $\frac{1}{d}$-integral if and only if $\mathcal{L}$ has the following *weak max-flow-min-cut property* (since the weak max-flow-min-cut property is closed under minors [10]): $\mathcal{L} = \{\emptyset\}$ or, for each $w \in \mathbb{Z}_+^E$, the program

$$\begin{array}{lll} \min & w^T x & \\ \text{subject to} & x(C) \geq 1 & \text{for all } C \in \mathcal{L} \\ & x_e \geq 0 & \text{for all } e \in E \end{array}$$

has an integer optimizing vector.
The clutter $\mathcal{L}$ is said to be *mengerian* if $\mathcal{L} = \{\emptyset\}$, or both the above program and its dual

$$\begin{array}{lll} \max & 1^T y & \\ \text{subject to} & \sum_{e \in C} y_C \leq w_e & \text{for } e \in E \\ & y_C \geq 0 & \text{for } C \in \mathcal{L} \end{array}$$

have integer optimizing vectors for all $w \in \mathbb{Z}_+^E$. Seymour [10] showed that a clutter $\mathcal{L} \neq \{\emptyset\}$ which is a matroid port is mengerian if and only if $\mathcal{L}$ is binary and does not have any Q_6 minor. Therefore, from Theorem 1.2, the class of the binary clutters which are box $\frac{1}{d}$-integral for some integer $d \geq 2$ is strictly contained in the class of mengerian binary clutters.

The characterization of the clutters with the weak max-flow-min-cut property is a hard and unsolved problem, even within the class of matroid ports (see [10], [4]).

We mention yet another equivalent definition for box $\frac{1}{d}$-integral clutters. Let $\mathcal{L}$ be a clutter on E and let F be a k-dimensional face ($k \geq 0$) of the polyhedron

$$Q(\mathcal{L}) := \{x \in \mathbb{R}_+^E : x(C) \geq 1 \text{ for all } C \in \mathcal{L}\}.$$

A subset $J \subseteq E$ is said to be *basic for the face* F if there exist $|E|-k$ equations $x(C_i) = 1$, with $C_i \in \mathcal{L}$ for $1 \leq i \leq |E|-k$, defining F and whose projections on $\mathbb{R}^J$ are linearly independent. Then, it is easy to check that $\mathcal{L}$ is box $\frac{1}{d}$-integral if and only if, for each k-dimensional face F of $Q(\mathcal{L})$ ($k \geq 0$), for each basic set $J \subseteq E$ for F and for each $x \in F$, $x_e \in \frac{1}{d}\mathbb{Z}$ for all $e \in J$ whenever $x_e \in \frac{1}{d}\mathbb{Z}$ for all $e \in E - J$. This definition corresponds to the "$\mathcal{F}$-property" considered (in blocking terms and in a slightly more general setting) by Nobili and Sassano ([8]). It expresses the fact that, not only all the vertices of $\mathcal{L}$ are $\frac{1}{d}$-integral, but also each face of $Q(\mathcal{L})$ contains, in the way mentioned above, a $\frac{1}{d}$-integral vector.

Let U_4^2 denote the matroid on four elements whose circuits are the sets $\{1,2,3\}$, $\{1,2,4\}$, $\{1,3,4\}$ and $\{2,3,4\}$. Then, its 4-port is the clutter C_3 consisting of the sets $\{1,2\}$, $\{1,3\}$ and $\{2,3\}$. It is easy to check that C_3 is box $\frac{1}{d}$-integral if and only if d is even.

PROPOSITION 1.3 *Let d be an odd integer and let $\mathcal{L}$ be a matroid port. If $\mathcal{L}$ is box $\frac{1}{d}$-integral, then $\mathcal{L}$ is a binary clutter.*

PROOF. Let $\mathcal{L}$ be the ℓ-port of a matroid $\mathcal{M}$. We can suppose that $\mathcal{M}$ is connected. Assume that $\mathcal{L}$ is box $\frac{1}{d}$-integral. Then, by Proposition 3.2, $\mathcal{L}$ does not have C_3 as a minor. Therefore, $\mathcal{M}$ does not have a minor U_4^2 using the element ℓ. This implies [3] that $\mathcal{M}$ does not have any minor U_4^2. Therefore, $\mathcal{M}$ is a binary matroid [15]. Hence, $\mathcal{L}$ is a binary clutter. ∎

In order to prove Theorem 1.2, it suffices to show the implications $(iii) \Longrightarrow (i)$ and $(i) \Longrightarrow (ii)$. The implication $(iii) \Longrightarrow (i)$ is implied by the following facts:
- box $\frac{1}{d}$-integrality is preserved under minors, see Proposition 3.2.
- Q_6 is not box $\frac{1}{d}$-integral, for each integer $d \geq 2$, see Proposition 3.3.
- Q_7 is not box $\frac{1}{d}$-integral, for each integer $d \geq 2$, see Proposition 3.4.

The most difficult part is to show the implication $(i) \Longrightarrow (ii)$. For this, we use as main tool a decomposition result for matroids without minor F_7^* using a given element ℓ (Tseng and Truemper [14], Truemper [12]), stated in Theorem 2.3.

The proof of Theorem 1.2 is presented in Sections 3 and 4. In Section 2, we recall some results about matroids and the decomposition result that we need here. We present in Section 5 some applications of our main result.

We use the following notation. Given a set A and elements $a \in A$, $b \notin A$, $A - a$, $A + b$ denote, respectively, $A - \{a\}$ and $A \cup \{b\}$. If x, y are two binary vectors, then $x \oplus y$ denotes the binary vector obtained by taking the componentwise sum of x and y modulo 2.

2 Preliminaries on matroids

We refer to [17], [13] for an introduction to matroids.

Representation matrix

Let $\mathcal{M}$ be a binary matroid on a set E, i.e. there exists a binary matrix M whose columns are indexed by E such that a subset of E is independent in $\mathcal{M}$ if and only if the corresponding subset of columns of M is linearly independent over the field $GF(2)$. Such a matrix M is called a *representation matrix* of $\mathcal{M}$.

Let X be a base of $\mathcal{M}$ and set $Y = E - X$. For $y \in Y$, let C_y denote the fundamental circuit of y in the base X, i.e. C_y is the unique circuit of $\mathcal{M}$ such that $y \in C_y$ and $C_y \subseteq X + y$. Let B denote the $|X| \times |Y|$ matrix whose columns are the incidence vectors of the sets $C_y - y$ for $y \in Y$. Then, the matrix $[I|B]$ is a representation matrix of $\mathcal{M}$ and B is then called a *partial representation matrix* of $\mathcal{M}$.

For $x \in X$, let Σ_x denote the fundamental cocircuit of x in the base X, i.e. Σ_x is the unique cocircuit of $\mathcal{M}$ such that $x \in \Sigma$ and $\Sigma \subseteq Y + x$. Then, the row of B indexed by x is the incidence vector of the set $\Sigma_x - x$.

For $y \in Y$ and $x \in C_y$, the set $X' = X - x + y$ is also a base of $\mathcal{M}$. The partial representation matrix B' of $\mathcal{M}$ in the base X' is easily obtained from B by *pivoting* with respect to the (x, y)-entry of B. Let $R_{x'}$, $x' \in X$, denote the rows of B, they are vectors in $\{0,1\}^Y$. Pivoting with respect to the (x, y)-entry of B amounts to replacing $R_{x'}$ by $R_{x'} \oplus R_x \oplus (1, 0, \ldots, 0)$ (where 1 is the y-position) for each $x' \in C_y$, $x' \neq x, y$.

Let $\mathcal{C}$ denote the family of circuits of $\mathcal{M}$. A set $C \subseteq E$ is called a *cycle* of $\mathcal{M}$ if $C = \emptyset$ or C is a disjoint union of circuits of $\mathcal{M}$. Equivalently, if M is a representation matrix of $\mathcal{M}$, the cycles are the subsets whose incidence vectors u satisfy $Mu \equiv 0 \pmod 2$.

Minors

Let Z be a subset of E. The matroid $\mathcal{M} \backslash Z$, obtained by *deletion* of Z, is the matroid on $E - Z$ whose family of circuits is $\mathcal{C} \backslash Z$. The matroid $\mathcal{M}/Z$, obtained by *contraction* of

Z, is the matroid on $E - Z$ whose circuits are the nonempty sets of $\mathcal{C}/Z$. A *minor* of $\mathcal{M}$ is obtained by a sequence of deletions and contractions. Every minor of $\mathcal{M}$ is of the form $\mathcal{M}\backslash Z/Z'$ for some disjoint subsets Z, Z' of E. Given $e \in E$, the minor $\mathcal{M}\backslash Z/Z'$ *uses the element* e if $e \notin Z \cup Z'$, i.e. e belongs to the groundset of $\mathcal{M}\backslash Z/Z'$.

Minors can be easily visualized on the partial representation matrix. Let B be the partial representation matrix of $\mathcal{M}$ corresponding to the base X. If $Z \subseteq X$, then the matrix obtained from B by deleting its rows indexed by Z is a partial representation matrix of $\mathcal{M}/Z$ and, if $Z \subseteq Y$, then the matrix obtained from B by deleting its columns indexed by Z is a partial representation matrix of $\mathcal{M}\backslash Z$.

k-sum

Let $\mathcal{M}_i$ be a binary matroid on E_i, for $i = 1, 2$. We define the binary matroid $\mathcal{M}$ on $E = E_1 \triangle E_2$ whose cycles are the subsets of E of the form $C_1 \triangle C_2$, where C_i is a cycle of $\mathcal{M}_i$ for $i = 1, 2$. We consider the cases:

• $E_1 \cap E_2 = \emptyset$, then $\mathcal{M}$ is called the 1-*sum* of $\mathcal{M}_1$ and $\mathcal{M}_2$

• $|E_1|, |E_2| \geq 2$, $E_1 \cap E_2 = \{e_0\}$ and e_0 is not a loop or a coloop of $\mathcal{M}_1$ or $\mathcal{M}_2$, then $\mathcal{M}$ is the 2-*sum* of $\mathcal{M}_1$ and $\mathcal{M}_2$.

k-separation

Let $r(.)$ denote the rank function of the matroid $\mathcal{M}$ on E. Let $k \geq 1$ be an integer. A *k-separation* of $\mathcal{M}$ is a partition (E_1, E_2) of the groudset E satisfying

$$\begin{cases} |E_1|, |E_2| \geq k \\ r(E_1) + r(E_2) \leq r(E) + k - 1 \end{cases}$$

When equality $r(E_1) + r(E_2) = r(E) + k - 1$ holds, the separation is called *strict*. The matroid $\mathcal{M}$ is said to be *k-connected* if it has no j-separation for $j \leq k - 1$. Throughout the paper, 2-connected will be abbreviated as *connected*.

If $\mathcal{M}$ has a strict k-separation (E_1, E_2), then it admits a partial representation matrix with a special form. Indeed, let X_2 be a maximal independent subset of E_2 and let $X_1 \subseteq E_1$ such that $X = X_1 \cup X_2$ is a base of $\mathcal{M}$, so $|X_1| = r(E_1) - k + 1$ and $|X_2| = r(E_2)$. The partial representation matrix B of $\mathcal{M}$ in the base X has the form shown in Figure 1.

Figure 1

The rank of the matrix D is equal to $k-1$.

In the case $k=1$ of a strict 1-separation, the matrix D is identically zero. Then, $\mathcal{M}$ is the 1-sum of $\mathcal{M}_1$ and $\mathcal{M}_2$.

In the case $k=2$ of a strict 2-separation, the matrix D has rank 1 and, thus, has the form shown in Figure 2.

Figure 2

So, the set $\tilde{Y}_1$ consists of the elements $y \in Y_1$ such that $X_1 + y$ is an independent set of $\mathcal{M}$ and, for $y \in \tilde{Y}_1$, the fundamental circuit of y in the base X is of the form $\tilde{X}_2 \cup A_y \cup \{y\}$ with $A_y \subseteq X_1$.

Given two elements $e_1 \in \tilde{X}_2$ and $e_2 \in \tilde{Y}_1$, we consider the matroids $\mathcal{M}_1 = \mathcal{M} / (X_2 - e_1) \setminus Y_2$ and $\mathcal{M}_2 = \mathcal{M}/X_1 \setminus (Y_1 - e_2)$ defined, respectively, on $E_1 \cup \{e_1, \ell\}$ and $E_2 \cup \{e_2, \ell\}$. It follows from the next Proposition 2.1 that $\mathcal{M}$ is the 2-sum of $\mathcal{M}_1$ and $\mathcal{M}_2$ (after renaming e_1 as e_0 in $\mathcal{M}_1$ and e_2 as e_0 in $\mathcal{M}_2$). A set $C \subseteq E$ is said to be *crossing* if $C \cap E_1 \neq \emptyset$ and $C \cap E_2 \neq \emptyset$.

PROPOSITION 2.1 *(i) Let C be a circuit of $\mathcal{M}$. Then,*
- *either $C \subseteq E_i$ and C is a circuit of $\mathcal{M}_i$, for some $i \in \{1,2\}$,*
- *or C is crossing and $(C \cap E_i) + e_i$ is a circuit of $\mathcal{M}_i$, for $i = 1$ and 2. Moreover, $(C \cap E_1) \cup \tilde{X}_2$ and $(C \cap E_2) \triangle \tilde{X}_2$ are circuits of $\mathcal{M}$.*

Every circuit of $\mathcal{M}_i$ arises in one of the two ways indicated above.
(ii) Let C, C' be two crossing circuits of $\mathcal{M}$, then $(C \cap E_i) \triangle (C' \cap E_j)$ is a cycle of $\mathcal{M}$ for any $i, j \in \{1,2\}$.

PROOF. (ii) follows directly from (i) and (i) is easy to check after observing that, for a circuit C of $\mathcal{M}$, C is crossing if and only if $|C \cap \tilde{Y}_1|$ is odd. ∎

In the case $k=3$ of a strict 3-separation, the matrix D has rank 2. Moreover, if $|E_1|, |E_2| \geq 4$ and $\mathcal{M}$ is 3-connected, it can be shown that $\mathcal{M}$ has a partial representation matrix B of the form shown in Figure 3, with $D_{12} = D_2 D_1$ (see [12]).

Figure 3

PROPOSITION 2.2 *Suppose $\mathcal{M}$ has a strict 3-separation (E_1, E_2) with $|E_1|$, $|E_2| \geq 4$ and consider the partial representation matrix of $\mathcal{M}$ from Figure 3. If $\{y, z, \ell\}$ is a circuit of the matroid $\mathcal{M}\backslash(X_1 - x)/(Y_1 - \{y, z\})$, then the partition $(E_1, E_2 - \ell)$ of $E - \ell$ is a strict 2-separation of the matroid $\mathcal{M}/\ell$.*

PROOF. Let a, b denote the rows of D_1 indexed, respectively, by e, f and let u, v denote the columns of D_2 indexed, respectively, by y, z. So, a, b are vectors indexed by the elements $y' \in Y_1 - \{y, z\}$ and u, v are indexed by the elements $x' \in X_2 - \{e, f\}$. Let w denote the vector whose components are the (x', ℓ)-entries, for $x' \in X_2 - \{e, f\}$, of the first column of B_2. Since the set $\{y, z, \ell)$ is a circuit of the matroid $\mathcal{M}\backslash(X_1 - x)/(Y_1 - \{y, z\})$, we deduce that $w = u \oplus v$.

The (e, ℓ)-entry of B is equal to 1, hence the set $X' = X - e + \ell$ is again a base of $\mathcal{M}$. Let B' denote the partial representation matrix of $\mathcal{M}$ in the base X'. So B' can be obtained from B by pivoting with respect to its (e, ℓ)-entry. Pivoting will affect only the rows of B indexed by $X_2 - e$. Let D' denote the submatrix of B' with row index set $X_2 - e + \ell$ and with column index set Y_1. It is not difficult to check that the row of D' indexed by f is the vector $(a \oplus b, 1, 1)$ and that each other row of D' indexed by some element of $X_2 - \{e, f\}$ is one of the two vectors $(a \oplus b, 1, 1)$ or $(0, \ldots, 0, 0, 0)$. Therefore, the submatrix of D' with row index set $X_2 - e$ has rank 1. This shows that the partition $(E_1, E_2 - \ell)$ of $E - \ell$ is a strict 2-separation of the matroid $\mathcal{M}/\ell$. ∎

Fano matroid

The *Fano matroid* F_7 is the matroid on $\{1,2,3,4,5,6,7\}$ whose circuits are the seven sets $\{1,2,3\}$, $\{1,4,7\}$, $\{1,5,6\}$, $\{2,4,6\}$, $\{2,5,7\}$, $\{3,4,5\}$ and $\{3,6,7\}$ (the lines of the Fano plane) together with their complements. The *dual Fano matroid* F_7^* is the dual of F_7, its circuits are $\{4,5,6,7\}$, $\{2,3,5,6\}$, $\{2,3,4,7\}$, $\{1,3,5,7\}$, $\{1,3,4,6\}$, $\{1,2,6,7\}$ and $\{1,2,4,5\}$ (the complements of the lines of the Fano plane).

By symmetry, there is only one port for F_7^*. The 7-port of F_7^* is the clutter Q_6, already defined earlier, consisting of the sets $\{4,5,6\}$, $\{2,3,4\}$, $\{1,3,5\}$ and $\{1,2,6\}$.

Observe that every one-element contraction of F_7 has a 2-separation. For example, the sets $\{1,4\}$ and $\{2,3,5,6\}$ form a strict 2-separation of $F_7/7$.

We also consider the *series-extension* F_7^+ of the Fano matroid F_7, obtained by adding a new element "8" in series with, say, the element "7", i.e. $\{7,8\}$ is a cocircuit of F_7^+. Hence, F_7^+ is the matroid defined on $\{1,2,3,4,5,6,7,8\}$ whose circuits are the sets C for which C is a circuit of F_7 with $7 \notin C$, and the sets $C \cup \{8\}$ for which C is a circuit of F_7 with $7 \in C$. Up to symmetry, there are two distinct ℓ-ports of F_7^+, depending whether ℓ is one of the two series elements $7,8$, or not. We denote by Q_7 the ℓ-port of F_7^+ when ℓ is a series element of F_7^+. Then, for $\ell = 8$, Q_7 consists of the sets $\{1,4,7\}$, $\{2,5,7\}$, $\{3,6,7\}$, $\{1,2,6,7\}$, $\{1,3,5,7\}$, $\{2,3,4,7\}$ and $\{4,5,6,7\}$, i.e. Q_7 consists of the circuits of F_7 containing the point 7.

We use the following facts about regular matroids ([13], [15], [17]). A matroid is *regular* if it does not have any F_7, F_7^*, or U_4^2 minor. Let $\mathcal{M}$ be a regular matroid and let $M = [I|B]$ be a binary matrix representing $\mathcal{M}$ over $GF(2)$. Then the 1's of B can be replaced by ± 1's so that the resulting matrix $\tilde{B}$ is totally unimodular, i.e. each square submatrix of $\tilde{B}$ has determinant $0, \pm 1$. Moreover, $\tilde{M} = [I|\tilde{B}]$ represents $\mathcal{M}$ over $\mathbb{R}$ and every binary vector x such that $Mx \equiv 0 \pmod 2$ corresponds to some $0,\pm 1$-vector y such that $\tilde{M}y = 0$, where y is obtained from x by replacing its 1's by ± 1's.

Decomposition result

The following decomposition result was proved by Tseng and Truemper ([14], Theorem 4.3); see also ([12], Theorem 1.3) and [13] for a detailed exposition.

THEOREM 2.3 *Let $\mathcal{M}$ be a matroid on the set $E \cup \{\ell\}$. Assume that $\mathcal{M}$ does not have any minor F_7^* using the element ℓ. Then, one of the following assertions holds.*
(i) $\mathcal{M}$ has a 1-separation.
(ii) $\mathcal{M}$ is 2-connected and has a 2-separation.
(iii) $\mathcal{M}$ is a regular matroid.
(iv) $\mathcal{M}$ is the Fano matroid F_7.
(v) $\mathcal{M}$ is 3-connected and has a 3-separation $(E_1, E_2 \cup \{\ell\})$ such that (E_1, E_2) is a strict 2-separation of $\mathcal{M}/\ell$.

REMARK 2.4 *Theorem 2.3 differs from Theorem 1.3 from [12] in the statement (v). However, the above formulation of (v) follows from Theorems 1.3 and 2.1 from [12] (the latter theorem states that the triple $\{y, z, \ell\}$ forms a circuit of $\mathcal{M}\backslash(X_1 - x)/(Y_1 - \{y, z\})$) and from the above Proposition 2.2.*

We will use this decomposition result in the following form.

THEOREM 2.5 *Let $\mathcal{M}$ be a binary matroid on the set $E \cup \{\ell\}$. Assume that $\mathcal{M}$ does not have any minor F_7^* using the element ℓ and that $\mathcal{M}$ does not have any minor F_7^+ using the element ℓ as a series element. Assume also that ℓ is not a coloop of $\mathcal{M}$. Then, one of the following assertions holds.*
(a) $\mathcal{M}/\ell$ has a 1-separation.
(b) $\mathcal{M}/\ell$ has a strict 2-separation.
(c) $\mathcal{M}$ is regular.

PROOF. We apply Theorem 2.3. The statement (iii) coincides with (c). (b) applies in the cases (iv) and (v). In the case (i), if $(E_1, E_2 \cup \{\ell\})$ is a 1-separation of $\mathcal{M}$, then (E_1, E_2) is a 1-separation of $\mathcal{M}/\ell$ since ℓ is not a coloop of $\mathcal{M}$; hence, (a) applies. We suppose finally that we are in the case (ii), i.e. $(E_1, E_2 \cup \{\ell\})$ is a strict 2-separation of $\mathcal{M}$. If $r_{\mathcal{M}}(E_1) = r_{\mathcal{M}/\ell}(E_1) + 1$, then (E_1, E_2) is a 1-separation of $\mathcal{M}/\ell$ and, thus, (a) applies. Otherwise, $r_{\mathcal{M}}(E_1) = r_{\mathcal{M}/\ell}(E_1)$, implying that $r_{\mathcal{M}/\ell}(E_1) + r_{\mathcal{M}/\ell}(E_2) = r_{\mathcal{M}/\ell}(E) + 1$; hence, in order to show that (b) applies, we need only to check that $|E_2| \geq 2$. Suppose, for contradiction, that $|E_2| = 1$, i.e. $E_2 = \{\ell'\}$. We deduce that $\{\ell, \ell'\}$ is a cocircuit of $\mathcal{M}$. Therefore, $\mathcal{M}$ can be seen as the series-extension of $\mathcal{M}/\ell$ obtained by adding ℓ in series with ℓ'. If $\mathcal{M}/\ell$ is regular, then $\mathcal{M}$ is regular too and, thus, (c) applies. Hence, we can suppose that $\mathcal{M}/\ell$ is 2-connected and not regular. It follows from [9] that $\mathcal{M}/\ell$ has a minor F_7 or F_7^* using ℓ'. It is easy to see that, if $\mathcal{M}/\ell$ has a minor F_7^* using ℓ', then $\mathcal{M}$ has a minor F_7^* using ℓ and, if $\mathcal{M}/\ell$ has a minor F_7 using ℓ', then $\mathcal{M}$ has a minor F_7^+ using ℓ as a series element. We obtain a contradiction in both cases. ∎

REMARK 2.6 *One can check that, under the conditions of Theorem 2.5 (i.e. $\mathcal{M}$ has no minor F_7^* using ℓ, no minor F_7^+ using ℓ as a series element and ℓ is not a coloop of $\mathcal{M}$), $\mathcal{M}/\ell$ is regular, or $\mathcal{M}$ has a 1-separation.*

Signed circuits

Let $\mathcal{M}$ be a binary matroid on $E \cup \{\ell\}$ and let $\mathcal{L}$ denote the ℓ-port of $\mathcal{M}$. A convenient way to refer to the members of $\mathcal{L}$ is in terms of odd circuits of $\mathcal{M}/\ell$ with respect to some signing. Given a set $\Sigma \subseteq E + \ell$, a subset $A \subseteq E$ is called Σ-*even* (resp. Σ-*odd*) if $|A \cap \Sigma|$ is even (resp. odd). It is immediate to check that

PROPOSITION 2.7 *Let Σ be a cocircuit of $\mathcal{M}$ such that $\ell \in \Sigma$ and let C be a subset of E. Then, $C \in \mathcal{L}$ if and only if C is a Σ-odd circuit of $\mathcal{M}/\ell$.*

3 Q_6, Q_7 and regular case

In this Section, we show the following results.
• It is sufficient to work with fully fractional vertices, see Proposition 3.1.
• Box $\frac{1}{d}$-integrality is preserved under minors, see Proposition 3.2.
• Q_6, the port of F_7^*, is not box $\frac{1}{d}$-integral for any integer $d \geq 2$, see Proposition 3.3.
• Q_7, the port of the series-extension of F_7 with respect to a series element, is not box $\frac{1}{d}$-integral for any integer $d \geq 2$, see Proposition 3.4.
• Any port of a regular matroid is box $\frac{1}{d}$-integral for each integer $d \geq 1$, see Theorem 3.5.

The following result is easy to check.

PROPOSITION 3.1 *Let $f \in E$, $I \subseteq E - f$, $a \in (\frac{1}{d}\mathbb{Z})^I$ and $x \in \mathbb{R}^{E-f}$. Then,*
(i) x belongs to (resp. is a vertex of) $Q(\mathcal{L}/\ell, a)$ if and only if $(x, 0)$ belongs to (resp. is a vertex of) $Q(\mathcal{L}, (a, 0))$.
(ii) x belongs to (resp. is a vertex of) $Q(\mathcal{L}\backslash\ell, a)$ if and only if $(x, 1)$ belongs to (resp. is a vertex of) $Q(\mathcal{L}, (a, 1))$.

As an immediate consequense, we have that

PROPOSITION 3.2 *Every minor of a box $\frac{1}{d}$-integral clutter is box $\frac{1}{d}$-integral.*

PROPOSITION 3.3 *The clutter Q_6 is not box $\frac{1}{d}$-integral, for any integer $d \geq 2$.*

PROOF. Consider the vector $u \in \mathbb{R}^6$ defined by $u_1 = 1 - \frac{1}{d}$, $u_2 = u_6 = \frac{1}{d}$, $u_3 = u_5 = \frac{1}{2d}$, $u_4 = 1 - \frac{3}{2d}$. Set $a_1 = 1 - \frac{1}{d}$, $a_2 = a_6 = \frac{1}{d}$. Then, u belongs to the polyhedron $Q(Q_6, a)$ and u is a vertex of it, since it satisfies the following six linearly independent equalities $u_1 + u_3 + u_5 = 1$, $u_2 + u_3 + u_4 = 1$, $u_4 + u_5 + u_6 = 1$, $u_1 = a_1$, $u_2 = a_2$ and $u_6 = a_6$. ∎

PROPOSITION 3.4 *The clutter Q_7 is not box $\frac{1}{d}$-integral, for any integer $d \geq 2$.*

PROOF. Consider the vector $u \in \mathbb{R}^7$ defined by $u_1 = u_3 = u_5 = \frac{1}{2d}$, $u_2 = u_4 = u_6 = \frac{1}{d}$, and $u_7 = 1 - \frac{3}{2d}$. Set $a_2 = a_4 = a_6 = \frac{1}{d}$. Then, u belongs to the polyhedron $Q(Q_7, a)$ and u is a vertex of it, since it satisfies the following seven linearly independent equalities $u_1 + u_4 + u_7 = 1$, $u_2 + u_5 + u_7 = 1$, $u_3 + u_6 + u_7 = 1$, $u_1 + u_3 + u_5 + u_7 = 1$, $u_2 = a_2$,

$u_4 = a_4$ and $u_6 = a_6$. ∎

THEOREM 3.5 *Let $\mathcal{L}$ be the port of a regular matroid. Then, $\mathcal{L}$ is box $\frac{1}{d}$-integral, for any integer $d \geq 1$.*

PROOF. Let $\mathcal{M}$ be a regular matroid on $E \cup \{\ell\}$ and let $\mathcal{L}$ be its ℓ-port. Since $\mathcal{M}$ is regular, we can find a totally unimodular matrix M which represents $\mathcal{M}$ over $\mathbb{R}$ and is of the form shown in Figure 4. We can suppose that the matrix A has full rank.

Figure 4

Moreover, each set $C \in \mathcal{L}$ corresponds to a vector $y_C \in \{0, 1, -1\}^E$ such that

$$\begin{cases} r^T y_C & = 1 \\ A y_C & = 0. \end{cases}$$

Each such y_C can be written as $y_C = y_C^1 - y_C^2$, where $y_C^1, y_C^2 \in \{0,1\}^E$ and their supports $\{e \in E : (y_C^1)_e = 1\}$, $\{e \in E : (y_C^2)_e = 1\}$ partition the set C.

We define the polyhedron $\mathcal{K}$ consisting of the vectors $(y_1, y_2) \in \mathbb{R}^E \times \mathbb{R}^E$ satisfying

$$\begin{cases} r^T y_1 - r^T y_2 & = 1 \\ A y_1 - A y_2 & = 0 \\ y_1, y_2 \geq 0. & \end{cases}$$

Clearly, $(y_C^1, y_C^2) \in \mathcal{K}$ for each $C \in \mathcal{L}$.

We state a preliminary result.

CLAIM 3.6 *Let $u \in \mathbb{R}_+^E$. Then, the following assertions hold.*
(i) $\min(u(C) : C \in \mathcal{L}) = \min(u^T y_1 + u^T y_2 : (y_1, y_2) \in \mathcal{K})$.

(ii) If the system $\begin{cases} r^T + \pi^T A & \leq u^T \\ -r^T - \pi^T A & \leq u^T \end{cases}$ *(in the variable π) is feasible, then $u(C) \geq 1$ holds for each $C \in \mathcal{L}$.*

Proof. (i) The first minimum is greater or equal to the second one since each $C \in \mathcal{L}$ corresponds to a pair $(y_C^1, y_C^2) \in \mathcal{K}$ such that $u(C) = u^T y_C^1 + u^T y_C^2$. Let (y_1, y_2) be a vertex of $\mathcal{K}$ at which the second minimum is attained. Clearly, the supports of y_1, y_2 are disjoint. Since the matrix M is totally unimodular, we deduce that $y_1, y_2 \in \{0,1\}^E$. Set $C = \{e \in E : (y_1)_e = 1 \text{ or } (y_2)_e = 1\}$. Then, $C \in \mathcal{L}$ and C corresponds to the vector $y_C = y_1 - y_2$ with $u^T y_1 + u^T y_2 = u(C)$. This shows that the second minimum is greater or equal to the first one.
(ii) If the system $\begin{cases} r^T + \pi^T A & \leq u^T \\ -r^T - \pi^T A & \leq u^T \end{cases}$ is feasible, then we have that $1 \leq \max(\rho : \rho r^T + \pi^T A \leq u^T,\ -\rho r^T - \pi^T A \leq u^T)$. Using linear programming duality, this implies that $\min(u^T y_1 + u^T y_2 : (y_1, y_2) \in \mathcal{K}) \geq 1$ and, therefore, by (i), $u(C) \geq 1$ for all $C \in \mathcal{L}$. ∎

Let I be a subset of E and let $a \in (\frac{1}{d}\mathbb{Z})^I$. Let $\tilde{Q}(\mathcal{L}, a)$ denote the polyhedron consisting of the vectors $(\pi, u) \in \mathbb{R}^m \times \mathbb{R}^E$ (m denoting the number of rows of the matrix A) satisfying

$$\begin{cases} \pi^T A & -u^T & \leq -r^T \\ -\pi^T A & -u^T & \leq r^T \\ & u_e & = a_e \quad \text{for } e \in I. \end{cases}$$

By Claim 3.6, $Q(\mathcal{L}, a)$ is the projection of $\tilde{Q}(\mathcal{L}, a)$ on the subspace $\mathbb{R}^E$. Let u be a vertex of $Q(\mathcal{L}, a)$. Hence, u is the projection of a vertex (π, u) of $\tilde{Q}(\mathcal{L}, a)$. By Proposition 3.1, we can suppose that $u_e > 0$ for all $e \in E$. Since $\tilde{Q}(\mathcal{L}, a)$ is invariant under the multiplication of some columns of the matrix $\left[\frac{r^T}{A}\right]$ by -1, we may assume that $\pi^T A + r^T \geq 0$. Therefore, (π, u) is a vertex of the polyhedron $\{(\pi, u) : \pi^T A - u^T \leq -r^T,\ u_e = a_e \text{ for } e \in I\}$. As the matrix defining it is totally unimodular, we deduce that (π, u) is $\frac{1}{d}$-integral and, thus, u is $\frac{1}{d}$-integral. (Note that the constraint matrix for $\tilde{Q}(\mathcal{L}, a)$ is not totally unimodular.) ∎

4 Proof of the main result

Let $\mathcal{M}$ be a binary matroid on $E \cup \{\ell\}$ and let $\mathcal{L}$ be the ℓ-port of $\mathcal{M}$, i.e. $\mathcal{L} = \{C \subseteq E : C + \ell \text{ is a circuit of } \mathcal{M}\}$. Let $d \geq 1$ be an integer. We assume that $\mathcal{L}$ does not have Q_6 or Q_7 as a minor. Hence, $\mathcal{M}$ does not have F_7^* as a minor using ℓ and $\mathcal{M}$ does not have F_7^+ as a minor using ℓ as a series element.

Our goal is to show that $\mathcal{L}$ is box $\frac{1}{d}$-integral. The proof is by induction on $|E| \geq 0$ and the main tool we use is Theorem 2.5.

The result holds for $|E| = 0$. Indeed, then ℓ is either a loop, yielding $\mathcal{L} = \{\emptyset\}$, or a coloop, yielding $\mathcal{L} = \emptyset$. In both cases, $\mathcal{L}$ is box $\frac{1}{d}$-integral.

We assume that the result holds for every groundset with less than $|E|$ elements, i.e. that every binary clutter without Q_6 or Q_7 minor on a set with less than $|E|$ elements is box $\frac{1}{d}$-integral.

We can suppose that ℓ is not a loop, nor a coloop of $\mathcal{M}$, i.e. that $\mathcal{L} \neq \{\emptyset\}, \emptyset$.

We know from Theorem 3.5 that $\mathcal{L}$ is box $\frac{1}{d}$-integral if $\mathcal{M}$ is regular. ¿From Theorem 2.5, we can assume that $\mathcal{M}$ has a 1-separation, or a strict 2-separation.

PROPOSITION 4.1 *If $\mathcal{M}/\ell$ has a 1-separation, then $\mathcal{L}$ is box $\frac{1}{d}$-integral.*

PROOF. Let (E_1, E_2) be a 1-separation of $\mathcal{M}/\ell$. Let $\mathcal{L}_1$ (resp. $\mathcal{L}_2$) denote the ℓ-port of the matroid $\mathcal{M}\backslash E_2$ (resp. $\mathcal{M}\backslash E_1$). Clearly, $\mathcal{L}_1 \cup \mathcal{L}_2 \subseteq \mathcal{L}$; in fact, $\mathcal{L} = \mathcal{L}_1 \cup \mathcal{L}_2$ is a partition of $\mathcal{L}$. By the induction assumption, $\mathcal{L}_1$ and $\mathcal{L}_2$ are box $\frac{1}{d}$-integral.

Given $a \in (\frac{1}{d}\mathbb{Z})^I$ where I is a subset of E, set $a_i = (a_e)_{e \in I \cap E_i}$, for $i = 1, 2$. Then, $Q(\mathcal{L}, a)$ is the cartesian product of $Q(\mathcal{L}_1, a_1)$ and $Q(\mathcal{L}_2, a_2)$, implying that all its vertices are $\frac{1}{d}$-integral. ∎

¿From now on, we assume that $\mathcal{M}/\ell$ is 2-connected and admits a 2-separation (E_1, E_2).

Let I be a subset of E, let $a \in (\frac{1}{d}\mathbb{Z})^I$ and let u be a vertex of $Q(\mathcal{L}, a)$. Our goal is to show that u is $\frac{1}{d}$-integral. From Proposition 3.1 and the induction hypothesis, we can suppose that $u_e \neq 0, 1$ for all $e \in E$. Call an inequality *tight* for u if it is satisfied at equality by u.

The inequalities defining $Q(\mathcal{L}, a)$ are of three types:
Type I: $x_e = a_e$ for $e \in I$.
Type II: $x(C) \geq 1$, for $C \in \mathcal{L}$ noncrossing (i.e. $C \subseteq E_i$ for $i \in \{1, 2\}$).
Type III: $x(C) \geq 1$, for $C \in \mathcal{L}$ crossing.

The case when no inequality of type III is tight for u is easy; the proof of the following result is analogous to that of Proposition 4.1.

PROPOSITION 4.2 *Assume that, for each crossing $C \in \mathcal{L}$, $u(C) > 1$ holds. Then, u is $\frac{1}{d}$-integral.*

We now suppose that there exists some crossing $C \in \mathcal{L}$ for which $u(C) = 1$ holds.

DEFINITION 4.3 *We call* path *every set of the form $C \cap E_i$, for $i \in \{1, 2\}$, where $C \in \mathcal{L}$ is crossing.*

Let Σ be a cocircuit of $\mathcal{M}$ which contains ℓ. Set

$$u_o = \min(u(P) : P \text{ is a path with } |P \cap \Sigma| \text{ odd})$$

$$u_e = \min(u(P) : P \text{ is a path with } |P \cap \Sigma| \text{ even}).$$

Both u_o, u_e are well defined.

PROPOSITION 4.4 *$u_o + u_e = 1$ holds. Moreover, for each tight crossing $C \in \mathcal{L}$ with, say, $C \cap E_1$ Σ-odd and $C \cap E_2$ Σ-even, then $u(C \cap E_1) = u_o$ and $u(C \cap E_2) = u_e$ holds.*

PROOF. Take $C \in \mathcal{L}$ crossing and tight. Then, $1 = u(C) = u(C \cap E_1) + u(C \cap E_2) \geq u_o + u_e$ holds. Conversely, suppose that $u_o = u(C \cap E_i)$ and $u_e = u(C' \cap E_j)$, where $C, C' \in \mathcal{L}$ are crossing with $C \cap E_i$ Σ-odd, $C' \cap E_j$ Σ-even and $i, j \in \{1, 2\}$. ¿From Proposition 2.1, $C'' = (C \cap E_i) \triangle (C' \cap E_j)$ is a cycle of $\mathcal{M}/\ell$. Hence, $C'' = \cup_h C_h$, where C_h are pairwise disjoint circuits of $\mathcal{M}/\ell$. Since C'' is Σ-odd, at least one of the C_h's is Σ-odd, i.e. belongs to $\mathcal{L}$. This implies that $u(C'') = \sum_h u(C_h) \geq 1$. Therefore, $u_o + u_e \geq 1$ holds. Hence, we have the equality $u_o + u_e = 1$. The last part of the Proposition follows immediately. ∎

Let $\mathcal{B}$ be a base of equalities for u, i.e. $\mathcal{B}$ is a maximal set of linearly independent inequalities chosen among the inequalities defining $Q(\mathcal{L}, a)$ that are satisfied at equality by u. Let $\mathcal{B}_i$ denote the subset of $\mathcal{B}$ consisting of the inequalities which are supported by E_i, for $i = 1, 2$. Hence, $\mathcal{B}_1 \cup \mathcal{B}_2$ consists of inequalities of Type I or II and $\mathcal{B} - \mathcal{B}_1 \cup \mathcal{B}_2$ of inequalities of Type III. We can partition $\mathcal{B} - \mathcal{B}_1 \cup \mathcal{B}_2$ as $\mathcal{B}_3 \cup \mathcal{B}_4$, where $\mathcal{B}_3$ consists of inequalities $x(C) \geq 1$ for $C \in \mathcal{L}$ crossing with $C \cap E_1$ Σ-odd, $C \cap E_2$ Σ-even, and $\mathcal{B}_4$ of such inequalities with $C \in \mathcal{L}$ crossing, $C \cap E_1$ Σ-even and $C \cap E_2$ Σ-odd.

PROPOSITION 4.5 *There exists a base $\mathcal{B}$ of equalities for u for which $\mathcal{B}_3 = \emptyset$ or $\mathcal{B}_4 = \emptyset$.*

PROOF. Let $\mathcal{B}$ be a base of equalities for u for which $|\mathcal{B}_1 \cup \mathcal{B}_2|$ is maximum. Suppose, for contradiction, that $\mathcal{B}_3 \neq \emptyset$ and $\mathcal{B}_4 \neq \emptyset$. Let $C, C' \in \mathcal{L}$ be crossing and yielding equalities of $\mathcal{B}$ with $C \cap E_1$, $C' \cap E_2$ Σ-even and $C \cap E_2$, $C' \cap E_1$ Σ-odd. By Proposition 2.1 (ii), $D_i := (C \cap E_i) \triangle (C' \cap E_i)$ is a cycle of $\mathcal{M}/\ell$, and D_i is Σ-odd by construction. Hence, $D_i = \sum_h C_h$ where the C_h's are circuits of $\mathcal{M}/\ell$ and at least one of them is Σ-odd. Using Proposition 4.4, we obtain that $1 = u_e + u_o \geq u(D_i) \geq 1$ which implies that D_i is a (noncrossing) circuit of $\mathcal{M}/\ell$ yielding a tight equality for u, for $i = 1, 2$, and $C \cap C' = \emptyset$. But $\mathcal{B}$ cannot contain both equations $x(D_1) = 1$ and $x(D_2) = 1$ since $C \cup C' = D_1 \cup D_2$. If $\mathcal{B}$ contains $x(D_1) = 1$ but not $x(D_2) = 1$, then, by replacing the equation $x(C') = 1$ by the equation $x(D_2) = 1$, we obtain a new base $\mathcal{B}'$ with $|\mathcal{B}'_1 \cup \mathcal{B}'_2| > |\mathcal{B}_1 \cup \mathcal{B}_2|$, contradicting the choice of $\mathcal{B}$. Otherwise, $\mathcal{B}$ contains none of the equations $x(D_1) = 1$, $x(D_2) = 1$. At least one of them can be added to $\mathcal{B}$ after deleting the equation $x(C') = 1$ and still preserve the linear independence. Again we obtain a contradiction with the maximality of $|\mathcal{B}_1 \cup \mathcal{B}_2|$. ∎

We can suppose, for instance, that we have a base $\mathcal{B}$ of equalities for u with $\mathcal{B}_4 = \emptyset$, $\mathcal{B}_3 \neq \emptyset$. (If both $\mathcal{B}_3$ and $\mathcal{B}_4$ are empty, we can conclude in the same way as in Proposition 4.2.) In matrix form, the system $\mathcal{B}$ can be written as $Px = \beta$, where β is the vector consisting of the right hand sides of the inequalities and the matrix P has the form shown in Figure 5.

Figure 5

Hence, there exists a tight equality $u(C^*) = 1$ where $C^* \in \mathcal{L}$ is crossing, $C^* \cap E_1$ is Σ-odd and $C^* \cap E_2$ is Σ-even. Then, we can find two elements $e_1 \in C^* \cap E_2$, $e_2 \in C^* \cap E_1$ with $e_1 \notin \Sigma$ and $e_2 \in \Sigma$ (after eventually changing the cocircuit Σ). (Indeed, let $e_2 \in C^* \cap E_1$, $e_1 \in C^* \cap E_2$ and let X be a base of $\mathcal{M}$ containing $(C^* - e_2) \cup \{\ell\}$. Let Σ' denote the fundamental cocircuit of ℓ in the base X; then, $e_2 \in \Sigma'$ since $C^* + \ell$ is the fundamental circuit of e_2 in the base X, and $e_1 \notin \Sigma'$ since $e_1 \in X$. Hence, it suffices to replace Σ by Σ'.)

Set $\mathcal{M}_1 = \mathcal{M}/((C^* \cap E_2) - e_1)\backslash(E_2 - C^*)$ and $\mathcal{M}_2 = \mathcal{M}/((C^* \cap E_1) - e_2)\backslash(E_1 - C^*)$, defined, respectively, on the sets $E_1 \cup \{e_1, \ell\}$ and $E_2 \cup \{e_2, \ell\}$. (Note that $\mathcal{M}_1$ coincides with $\mathcal{M}/(X_2 - e_1)\backslash Y_2$ and $\mathcal{M}_2$ coincides with $\mathcal{M}/X_1\backslash(Y_1 - e_2)$, where $X_i = X \cap E_i$, $Y_i = E_i - X_i$ for $i = 1, 2$. Also, $\mathcal{M}/\ell$ is the 2-sum of $\mathcal{M}_1/\ell$ and $\mathcal{M}_2/\ell$. Recall Section 2.)

Let $\mathcal{L}_i$ denote the ℓ-port of $\mathcal{M}_i$. By the induction assumption, $\mathcal{L}_i$ is box $\frac{1}{d}$-integral, for $i = 1, 2$.

Let u_i denote the projection of u on $\mathbb{R}^{E_i}$ and set $a_i = (a_e)_{e \in I \cap E_i}$, for $i = 1, 2$. We define $u_i^* \in \mathbb{R}^{E_i + e_i}$ by

$$\begin{cases} u_i^*(e) = u_i(e) \text{ for } e \in E_i, i = 1, 2, \\ u_1^*(e_1) = u_e, \\ u_2^*(e_2) = u_o. \end{cases}$$

PROPOSITION 4.6 *$u_i^* \in Q(\mathcal{L}_i, a_i)$, for $i = 1, 2$.*

PROOF. Take $C \in \mathcal{L}_i$. By Proposition 2.1 (i), either $C \in \mathcal{L}$ and, thus, $u_i^*(C) = u(C) \geq 1$, or $C = C' \cap E_i + e_i$ for some crossing circuit C' of $\mathcal{M}/\ell$. Say $i = 1$. Then, $C' \cap E_1$ is Σ-odd, since C is Σ-odd and $e_1 \notin \Sigma$. By Proposition 2.1 (ii), $(C' \cap E_1) \triangle (C^* \cap E_2)$ is a cycle of $\mathcal{M}/\ell$ and it is Σ-odd since $C^* \cap E_2$ is Σ-even. Hence, $u(C' \cap E_1) + u(C^* \cap E_2) \geq 1$ which, together with $u(C^* \cap E_2) = u_e$, implies that $u(C' \cap E_1) \geq 1 - u_e = u_o$. Therefore, $u_1^*(C) = u(C' \cap E_i) + u_e \geq u_o + u_e = 1$. The case $i = 2$ is identical. ∎

We construct the set $\mathcal{B}^{(i)}$ of equalities for u_i^* consisting of

- the equalities of $\mathcal{B}_i$,
- the equalities $x((C \cap E_i) + e_i) = 1$, one for each equality $x(C) = 1$ of $\mathcal{B}_3$.

All equalities of $\mathcal{B}^{(i)}$ arise from those defining $Q(\mathcal{L}_i, a_i)$. Indeed, by Proposition 2.1, if $C \in \mathcal{L}$ with $C \subseteq E_i$, then $C \in \mathcal{L}_i$ and, if $C \in \mathcal{L}$ is crossing, then $(C \cap E_i) + e_i \in \mathcal{L}_i$, for $i = 1, 2$.

PROPOSITION 4.7 *The set $\mathcal{B}^{(i)}$ has rank $|E_i| + 1$, for at least one index $i \in \{1, 2\}$.*

PROOF. We show that one of the two matrices from Figures 6 and 7 below has full rank $|E_i| + 1$.

Figure 6

Figure 7

This follows from the fact that the matrix displayed in Figure 8 has full rank $|E| + 2$; indeed, it can be obtained by row and column manipulations from the full rank matrix displayed in Figure 9. ∎

Figure 8

Figure 9

Suppose, for example, that $\mathcal{B}^{(1)}$ has full rank. This implies that u_1^* is a vertex of $Q(\mathcal{L}_1, a_1)$ and, thus, u_1^* is $\frac{1}{d}$-integral, since $\mathcal{L}_1$ is box $\frac{1}{d}$-integral. In particular, u_e is $\frac{1}{d}$-integral, implying that $u_o = 1 - u_e$ is $\frac{1}{d}$-integral. If we introduce the constraint $x(e_2) = u_o$, then u_2^* becomes a vertex of the polytope $Q(\mathcal{L}_2, a_2) \cap \{x : x(e_2) = u_o\}$ and, thus, u_2^* is $\frac{1}{d}$-integral.

This shows that u is $\frac{1}{d}$-integral, concluding the proof. ∎

5 Applications for graphs

A *signed graph* is a pair (G, Σ), where $G = (V, E)$ is a graph and Σ is a subset of the edge set E of G. The edges in Σ are called *odd* and the other edges *even*. An *odd circuit* C in (G, Σ) is a circuit C of G such that $|C \cap \Sigma|$ is odd. If $\delta(U)$ is a cut in G, then the two signed graphs (G, Σ) and $(G, \Sigma \triangle \delta(U))$ have the same collection of odd circuits. The operation $\Sigma \longrightarrow \Sigma \triangle \delta(U)$ is called *resigning* (by the cut $\delta(U)$). We say that (G, Σ) *reduces* to (G', Σ') if (G', Σ') can be obtained from (G, Σ) by a sequence of the following operations:

- deleting an edge of G (and Σ),
- contracting an even edge of G,
- resigning.

The collection of odd circuits of a signed graph is a binary clutter. Indeed, given a signed graph (G,Σ), let $\mathcal{S}(G,\Sigma)$ denote the binary matroid on $\{\ell\}\cup E$ represented over $GF(2)$ by the matrix $[\frac{1\ |\ \sigma}{0\ |\ M_G}]$, where M_G is the node-edge incidence matrix of G and σ is the incidence vector of the set Σ. Clearly, the ℓ-port of $\mathcal{S}(G,\Sigma)$ coincides with the family of odd circuits of (G,Σ). In particular, the collection of odd circuits of the signed graph $(K_4, E(K_4))$, i.e. K_4 with all edges odd, is the clutter Q_6, i.e. $\mathcal{S}(K_4,E(K_4))$ is F_7^*. One can check that (G,Σ) does not reduce to $(K_4,E(K_4))$ if and only if $\mathcal{S}(G,\Sigma)$ does not have an F_7^* minor using the element ℓ. Moreover, $\mathcal{S}(G,\Sigma)$ does not have any minor F_7^+ using ℓ as a series element, else F_7 would be a minor of the graphic matroid $\mathcal{M}(G)=\mathcal{S}(G,\Sigma)/\ell$. (See [5] for details.)

The following result is an immediate application of Theorem 1.2.

THEOREM 5.1 *Let (G,Σ) be a signed graph and let $\mathcal{L}$ denote its collection of odd circuits. The following assertions are equivalent.*
(i) (G,Σ) does not reduce to $(K_4,E(K_4))$.
(ii) $\mathcal{L}$ is box $\frac{1}{d}$-integral for any integer $d\geq 1$.
(iii) $\mathcal{L}$ is box $\frac{1}{d}$-integral for some integer $d\geq 2$.

Given a graph $G=(V,E)$, we consider the polytope

$$S(G)=\{x\in\mathbb{R}^E:\ \begin{array}{ll} x(F)-x(C-F)\leq |F|-1 & (C \text{ circuit of } G, F\subseteq C, |F| \text{ odd}),\\ 0\leq x_e\leq 1 & (e\in E)\}.\end{array}$$

The polytope $S(G)$ is a relaxation of the cut polytope $P(G)$ (defined as the convex hull of the incidence vectors of the cuts of G). In general, $S(G)$ has fractional vertices. In fact, the $0,1$-vertices of $S(G)$ are the incidence vectors of the cuts of G, and $S(G)$ has only integral vertices, i.e. $S(G)=P(G)$, if and only if G is not contractible to K_5 [2]. The fractional vertices of $S(G)$ have been studied in [6], [7].

The case $d=3$ of the following Theorem 5.2 was proved in [7]. We will show how Theorem 5.2 follows from Theorem 5.1.

THEOREM 5.2 *Let $G=(V,E)$ be a graph. The following assertions are equivalent.*
(i) G is series parallel, i.e. G is not contractible to K_4.
(ii) For each $I\subseteq E$ and $a\in(\frac{1}{d}\mathbb{Z})^I$, all the vertices of the polytope $S(G)\cap\{x : x_e = a_e$ for $e\in I\}$ are $\frac{1}{d}$-integral, for any integer $d\geq 1$.
(iii) For each $I\subseteq E$ and $a\in(\frac{1}{d}\mathbb{Z})^I$, all the vertices of the polytope $S(G)\cap\{x : x_e = a_e$ for $e\in I\}$ are $\frac{1}{d}$-integral, for some integer $d\geq 2$.

PROOF. Let $G'=(V,E\cup E')$ denote the graph obtained from G by adding an edge e' in parallel with each edge e of G. We consider the signed graph (G',E'), where the edges of

E are even and those of E' are odd. It is easy to see that G is series parallel if and only if (G', E') does not reduce to $(K_4, E(K_4))$. Let $\mathcal{L}'$ denote the collection of odd circuits of (G', E'). From Theorem 5.1, $\mathcal{L}'$ is box $\frac{1}{d}$-integral if G is series parallel.

For $x \in \mathbb{R}^E$, define $x' \in \mathbb{R}^{E'}$ by $x'_{e'} = 1 - x_e$ for $e \in E$ and, for $a \in (\frac{1}{d}\mathbb{Z})^I$ with $I \subseteq E$, set $a'_{e'} = 1 - a_e$ for $e \in I$.
Observe that $\mathcal{S}(G) \cap \{x : x_e = a_e \text{ for } e \in I\} = \{x : (x, x') \in Q(\mathcal{L}', (a, a'))\}$. As $\{e, e'\} \in \mathcal{L}'$ for each $e \in E$, $Q(\mathcal{L}', (a, a')) \cap \{(x, y) \in \mathbb{R}^E \times \mathbb{R}^{E'} : y_{e'} = 1 - x_e \text{ for } e \in E\}$ is a face of $Q(\mathcal{L}', (a, a'))$. Therefore, $\mathcal{S}(G) \cap \{x : x_e = a_e \text{ for } e \in I\}$ is the projection of a face of $Q(\mathcal{L}', (a, a'))$. Hence, all its vertices are $\frac{1}{d}$-integral if G is series parallel. This proves $(i) \Longrightarrow (ii)$.
It is easy to check that (iii) is closed under graph minors. Moreover, K_4 does not have the property (iii). Indeed, consider K_4 with its edges labeled $1, 2, 3, 4, 5, 6$ in such a way that the triangles of K_4 are $\{1, 2, 6\}$, $\{1, 3, 5\}$, $\{2, 3, 4\}$, $\{4, 5, 6\}$ (i.e. the members of Q_6). Set $x_2 = x_4 = x_6 = \frac{1}{d}$ and $x_1 = x_3 = x_5 = \frac{1}{2d}$. Then, x is a vertex of the polytope $S(K_4) \cap \{x : x_i = \frac{1}{d} \text{ for } i = 2, 4, 6\}$ which is not $\frac{1}{d}$-integral. This shows $(iii) \Longrightarrow (i)$. ∎

More generally, given a binary matroid $\mathcal{M}$ on a set E, consider the polytope $\mathcal{S}(\mathcal{M})$ in $\mathbb{R}^E$ defined by the inequalities $0 \leq x_e \leq 1$ for $e \in E$, and $x(F) - x(C - F) \leq |F| - 1$ for $F \subseteq C$ with $|F|$ odd and C circuit of $\mathcal{M}$. Hence, $S(\mathcal{M})$ coincides with $S(G)$ when $\mathcal{M}$ is the graphic matroid $\mathcal{M}(G)$ of G. The $0,1$-vertices of $S(\mathcal{M})$ are the incidence vectors of the cocycles of $\mathcal{M}$. The matroids $\mathcal{M}$ for which all vertices of $S(\mathcal{M})$ are integral have been characterized in [1] using a result of [11]. A natural question to ask is what are the matroids $\mathcal{M}$ for which $S(\mathcal{M})$ is box $\frac{1}{d}$-integral. Actually, this class is not larger than in the graphic case.

To see this, observe that $F_7^*/\ell = \mathcal{M}(K_4)$ and that $F_7^+/\ell = F_7$ has an $\mathcal{M}(K_4)$ minor. On the other hand, a binary matroid $\mathcal{M}$ has no $\mathcal{M}(K_4)$ minor if and only if $\mathcal{M}$ is the graphic matroid of a series parallel graph. The latter follows easily from Tutte's forbidden minor characterization of graphic matroids ([16]).

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