

Scheduling and compiling rate-synchronous programs with end-to-end latency constraints

Timothy Bourke

with Vincent Bregeon (Airbus) and Marc Pouzet

[Bourke, Bregeon, and Pouzet (2023): Scheduling and Compiling Rate-Synchronous Programs with End-to-End Latency Constraints]

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17 October 2023, Systèmes réactifs synchrones MPRI 2-23-1

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 - » `read` data from sensors via a bus,
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Airbus project “All-in-Lustre”

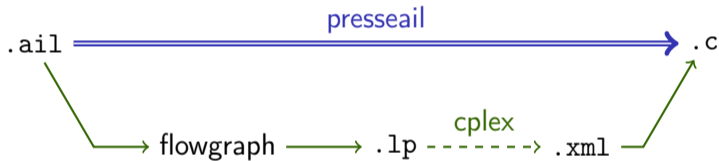
- *Original system*: $\approx 5\,000$ Lustre nodes
+ separate constraints on order
- *Desired system*: a **single Lustre program** with features for periods and end-to-end latencies.
- Nodes at 10ms, 20ms, 40ms, and 120ms.
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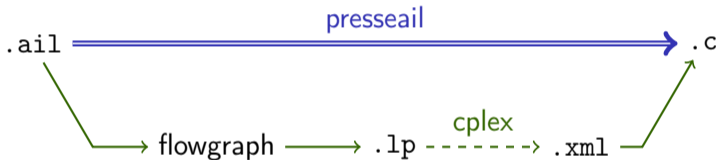
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- *Implementation*: sequential code, period = 5ms
- **Workload already chopped up into small pieces.**
- **Each node loops in < 5 ms.**

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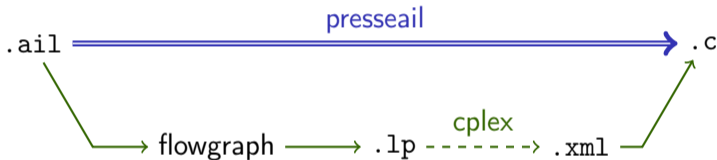
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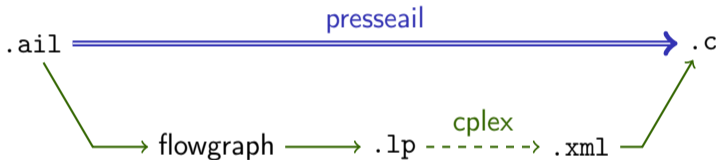
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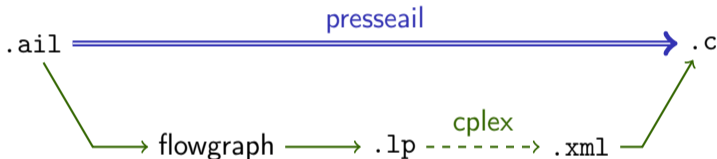


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- Vertex = node
- Arc from producer to consumer
- Independent of source language
- Data dependencies
- Load balancing
- End-to-end latency

Slow flows

```
resource cpu : int;

node read() returns (y:int);
node write(x:int) returns ();
node filter(x:int) returns (y:int);

node main() returns ()
var s0, s1, s2, s3 : int :: 1/3;
let
    s0 = read();
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    s2 = filter(s1);
    s3 = s1 + s2;
    () = write(s3);
tel
```

```
$ presseail example1.ail -v --glpk --print
```

- Declare variables of rate $1/3$ (period = 3)
- Calculate each once every three cycles

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- The 5 calculations here are **synchronous** relative to the period even if they are **not necessarily simultaneous** relative to the base clock
- $s3 = s1 + s2$ is well clocked since $s1 :: 1/3$, $s2 :: 1/3$, and $s3 :: 1/3$.

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- $s_3 = s_1 + s_2$ is well clocked since $s_1 :: 1/3$, $s_2 :: 1/3$, and $s_3 :: 1/3$.
- Causality applies 'across' a **period** and 'within' an **instant**: $s_0 \rightarrow s_1 \rightarrow s_2 \rightarrow s_3 \rightarrow ()$

Changing speeds: 1

```
resource cpu : int

node filter(x : int)
  returns (y : int);

node main(s0 : int)
  returns (s4 : int)
  var s1, s2 : int :: 1/3;
      s3 : int :: 1/3 last = 0;
  let
    s1 = filter(s0 when (0 % 3));
    s2 = filter(s1);
    s3 = filter(s2);
    s4 = current(s3, (2 % 3));
  tel
```

```
$ presseail example2.ail --glpk --compile 1
```

- `x when c`
 - » `c` is for '(sampling) choice'
 - » sub-sampling of a stream
 - » fast-to-slow rate change
- `current(x, c)`
 - » stutter stream elements
 - » must declare an initial `last` value
 - » slow-to-fast rate change

`y = merge c x ((0 fby y) when not c)`

$r = w$ when $(i \% n)$

- $(i \% n)$: take the i th of every n elements.
- n is the rate of w relative to r
E.g., for $w :: 1/4$ and $r :: 1/8$, n is 2.
- It can be deduced from the clocks, but is useful for readability.
- It implies a lower bound on the scheduling of the equation.

Changing speeds: 2

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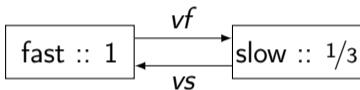
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- It implies a lower bound on the scheduling of the equation.
- Write $(? \% n)$ if we don't care when values are sampled/updated.
- The schedule decides when sampling/updating occur; fixed at compile time.

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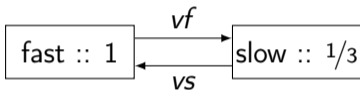
Rate-synchronous Model



```
node eg1() returns ()
var vf : int :: 1;
    n : int :: 1 last = 0;
    vs : int :: 1/3 last = 0;
let
    vf = n + current(vs, (2 % 3));
    n = (last n) + 1;
    vs = (vf when (1 % 3)) + 5;
tel
```

<i>vf</i>	1	2	10	11	12	23	24	25	39	...
<i>n</i>	1	2	3	4	5	6	7	8	9	...
<i>vs</i>	7		17			30			...	

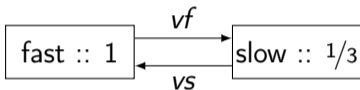
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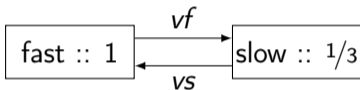


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Red arrows in the table indicate dependencies: from `vs` at index 2 to `vf` at index 2, and from `vs` at index 2 to `vf` at index 3.

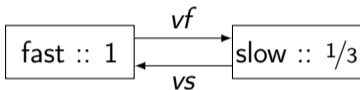
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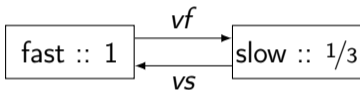
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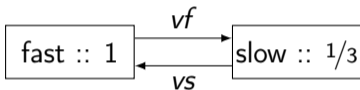
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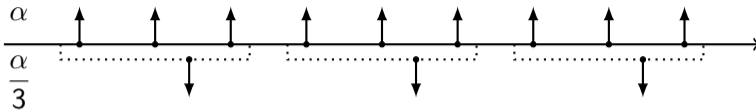
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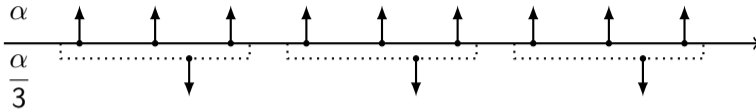
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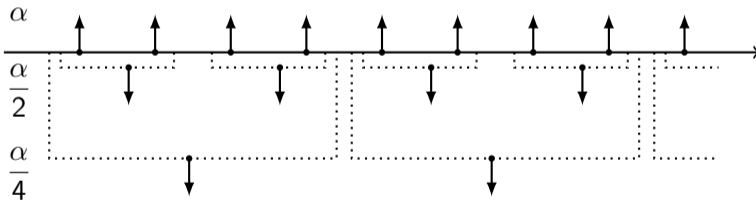


One slow tick is synchronous with three fast ones.

Rate-synchronous Model



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- Calculations are **synchronous** relative to their periods but **not necessarily simultaneous** relative to execution cycles
- The compiler assigns computations to phases, buffering values if necessary

Syntax

$eq ::= x = e \mid x^* = f(e^*)$

$e ::= c \mid x \mid \diamond e \mid e \oplus e \mid \text{if } e \text{ then } e \text{ else } e \mid \text{last } x$
 $\mid x \text{ when } s \mid (\text{last } x) \text{ when } s \mid \text{current}(x, s)$

$s ::= (c \% c) \mid (? \% c)$

$p ::= (d ;)^*$

$d ::= \text{resource } x : ty$

$\mid \text{node } f((x : ty ;)^*) \text{ returns } ((x : ty ;)^*) \text{ requires } ((x = c ;)^*)$

$\mid \text{node } f((x : ty :: ck [\text{last} = c] ;)^*) \text{ returns } ((x : ty :: ck [\text{last} = c] ;)^*)$

$\text{var } (x : ty :: ck [\text{last} = c] ;)^* \text{let } (((\text{pragmas } eq) \mid cst) ;)^+ \text{tel}$

$\text{pragmas} ::= [\text{label}(x)] [\text{phase}(c \% c)]$

$cst ::= \text{resource balance } x$

$\mid \text{resource } x \text{ rel } c$

$\mid \text{latency } (\text{exists} \mid \text{forward} \mid \text{backward}) \text{ rel } c (x, x(, x)^*)$

$\text{rel} ::= \leq \mid < \mid = \mid > \mid \geq$

Valid programs are defined by clock typing

$$\frac{e_1 :: 1/n \quad e_2 :: 1/n}{e_1 \oplus e_2 :: 1/n}$$

$$\frac{x :: 1/n}{\text{last } x :: 1/n}$$

$$\frac{x :: 1/m}{x \text{ when } (\cdot \% n) :: 1/mn}$$

$$\frac{x :: 1/mn}{\text{current}(x, (\cdot \% n)) :: 1/m}$$

- No phase offsets in clock types, unlike

- » Prelude: `rate(100, 0)`

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- Generated code: phase offsets implement data dependencies.

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$$\llbracket e_1 \oplus e_2 \rrbracket (i) = \llbracket e_1 \rrbracket (i) \oplus \llbracket e_2 \rrbracket (i)$$

$$\llbracket \text{last } x \rrbracket (i) = \begin{cases} x_{-1} & \text{if } i = 0 \\ \llbracket x \rrbracket (i - 1) & \text{otherwise} \end{cases}$$

$$\llbracket x \text{ when } (s \% n) \rrbracket (i) = \llbracket x \rrbracket (n \cdot i + s)$$

$$\llbracket \text{current}(x, (s \% n)) \rrbracket (i) = \begin{cases} x_{-1} & \text{if } i < s \\ \llbracket x \rrbracket (\lfloor i - s / n \rfloor) & \text{otherwise} \end{cases}$$

- Recursive equations on streams: $\mathbb{N} \rightarrow \mathbb{V}$
- x_{-1} is the initial last value
- No explicit presence or absence
- Cf. Prelude (tagged-signal model)

Declare and constrain resources

```
resource cpu : int
```

```
node read() returns (y:int);  
node write(x:int) returns ();  
node filter(x:int) returns (y:int)  
  requires (cpu = 4);
```

```
node main() returns ()  
var s0, s1, s2, s3 : int :: 1/3;  
let
```

```
  resource cpu <= 4;  
  s0 = read();  
  s1 = filter(s0);  
  s2 = filter(s1);  
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  () = write(s3);
```

```
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- Declare *named weights* to represent resources required per cycle
 - » Simple proxies for worst-case execution time
 - » Network bus accesses
- Use to constrain scheduling
- normally: `resource balance cpu`

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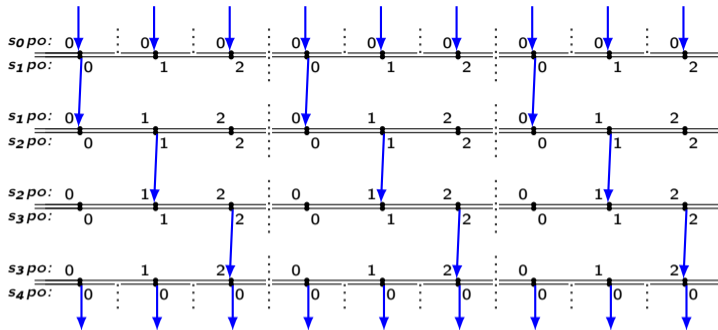
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- Declare *named weights* to represent resources required per cycle
 - » Simple proxies for worst-case execution time
 - » Network bus accesses
- Use to constrain scheduling
 - normally: `resource balance` `cpu`
 - Trade-off *resource balancing* against *latency*:
`latency_chain` `<= 0 (s0 -> s1 -> s2 -> s3);`

Macro-scheduling of equations

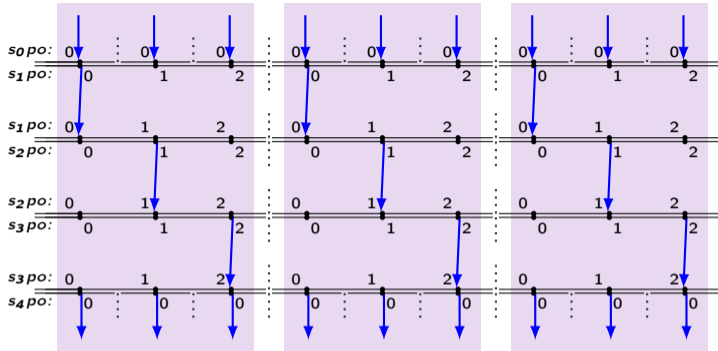
- Label each equation, scheduling assigns a **phase offset**
 - » Lustre with annotations as an ersatz intermediate language
 - » `label(filter_0) phase(1 % 3) s2 = filter(s1);`
- Phase offsets are constrained by
 - » Data dependencies in the source program
 - » Resource constraints
 - » Latency constraints. . .
- Phase offset (and latency) are implementation details
 - » They are relative to the base rate, not the equation rate
 - » Program semantics is independent of phase offsets



```

node main (s0 : int) returns (s4 : int)
var s1, s2 : int :: 1 / 3,
    s3 : int :: 1 / 3 last = 0;
let
  label(filter)    phase(0 % 3) s1 = filter(s0 when (0 % 3));
  label(filter_0)  phase(1 % 3) s2 = filter(s1);
  label(filter_1)  phase(2 % 3) s3 = filter(s2);
  label(s4_2)      phase(0 % 1) s4 = current(s3, (2 % 3));
tel

```



```

node main (s0 : int) returns (s4 : int)
var s1, s2 : int :: 1 / 3,
    s3 : int :: 1 / 3 last = 0;
let
  label(filter)    phase(0 % 3) s1 = filter(s0 when (0 % 3));
  label(filter_0)  phase(1 % 3) s2 = filter(s1);
  label(filter_1)  phase(2 % 3) s3 = filter(s2);
  label(s4_2)      phase(0 % 1) s4 = current(s3, (2 % 3));
tel

```

Usual Workflow

1. `$ presseail example2.ail --write-lp example2.lp`
writes the scheduling constraints to a file
2. Call `cplex`
3. `$ presseail example2.ail --read-sol example2.sol --compile 1`
reads the solution and generates code

Usual Workflow

1. `$ presseail example2.ail --write-lp example2.lp`
writes the scheduling constraints to a file
2. Call `cplex`
3. `$ presseail example2.ail --read-sol example2.sol --compile 1`
reads the solution and generates code

Testing simple examples

- `$ presseail example2.ail --glpk --compile 1`

ILP Problem

Maximize

obj: $x_1 + 2x_2 + 3x_3 + x_4$

Subject To

c1: $-x_1 + x_2 + x_3 + 10x_4 \leq 20$

c2: $x_1 - 3x_2 + x_3 \leq 30$

c3: $x_2 - 3.5x_4 = 0$

Bounds

$0 \leq x_1 \leq 40$

$2 \leq x_4 \leq 3$

General

x_4

End

- LP File Format Sections

- » 1. Minimize / Maximize: objective function
- » 2. Subject to: list of constraints
- » 3. Bounds: optional bounds on variables
- » 4. General: list of integer variables, **variables default to 'continuous'**
- » 5. Binary: $0 \leq$ integer variables ≤ 1
- » 6. End

- Constraints:

- » (*optional*) label:
- » sum of terms \leq constant (*also* \geq , *etc.*)
- » each term pairs a constant with a variable

Minimize

rmax.equ

Subject to

pw.def0.filter: pw.0.filter + pw.1.filter + pw.2.filter = 1

pw.def1.filter: 2 pw.2.filter + pw.1.filter - p.filter = 0

...

depd.wr.p.read.p.filter_5: p.filter - p.read \geq 0

...

rbnd.cpu_8: 5 pw.0.filter_1 + 5 pw.0.filter_0 + 5 pw.0.filter \leq 8

rbnd.cpu_7: 5 pw.1.filter_1 + 5 pw.1.filter_0 + 5 pw.1.filter \leq 8

rbnd.cpu_6: 5 pw.2.filter_1 + 5 pw.2.filter_0 + 5 pw.2.filter \leq 8

Bounds

0 \leq p.read $<$ 3

0 \leq p.filter $<$ 3

...

General

p.read p.filter ...

Binary

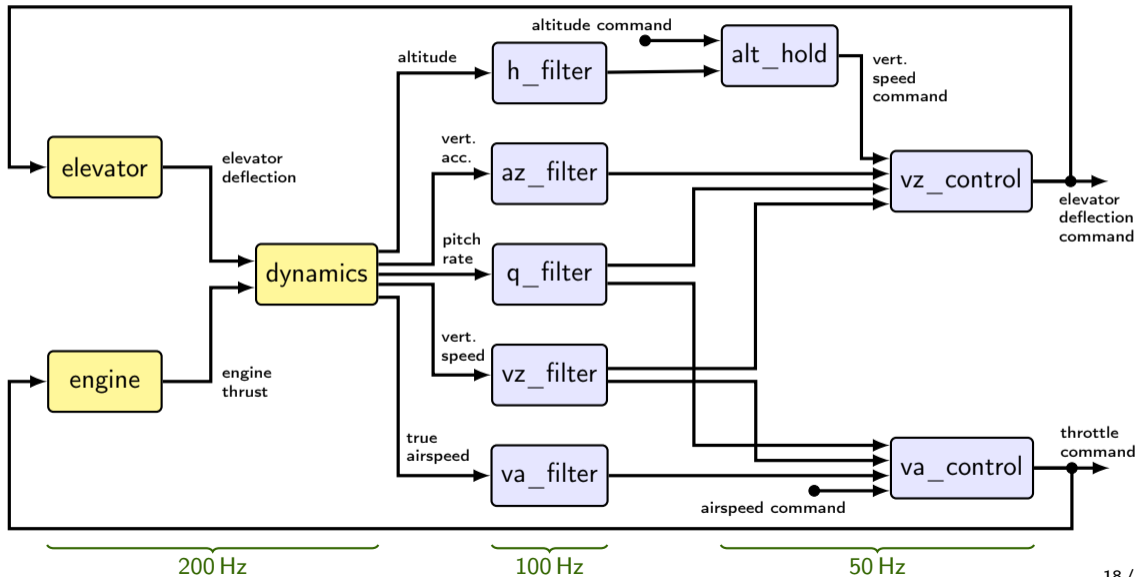
pw.0.read pw.1.read pw.2.read pw.0.filter ...

End

- Language [Forget, Boniol, Lesens, and Pagetti (2010):
A Real-Time Architecture Design Language
for Multi-Rate Embedded Control Systems] and compiler [Pagetti, Forget, Boniol, Cordovilla, and
Lesens (2011): Multi-task implementation
of multi-periodic synchronous programs]
- Extend Lustre with task periods/phases and WCET.
- Compose real-time primitives to express communication patterns.
- Generate and schedule a set of real-time tasks
 - » WCET, release times, deadlines
 - » Adapt existing scheduling algorithms to respect data dependencies
- “Don’t Care” [Wyss, Boniol, Forget, and Pagetti (2012): A Synchronous Language
with Partial Delay Specification for Real-Time Systems Programming],
Let the compiler decide if `c dc x (c fby? x)` is
 - » `c fby x`
 - » `x`

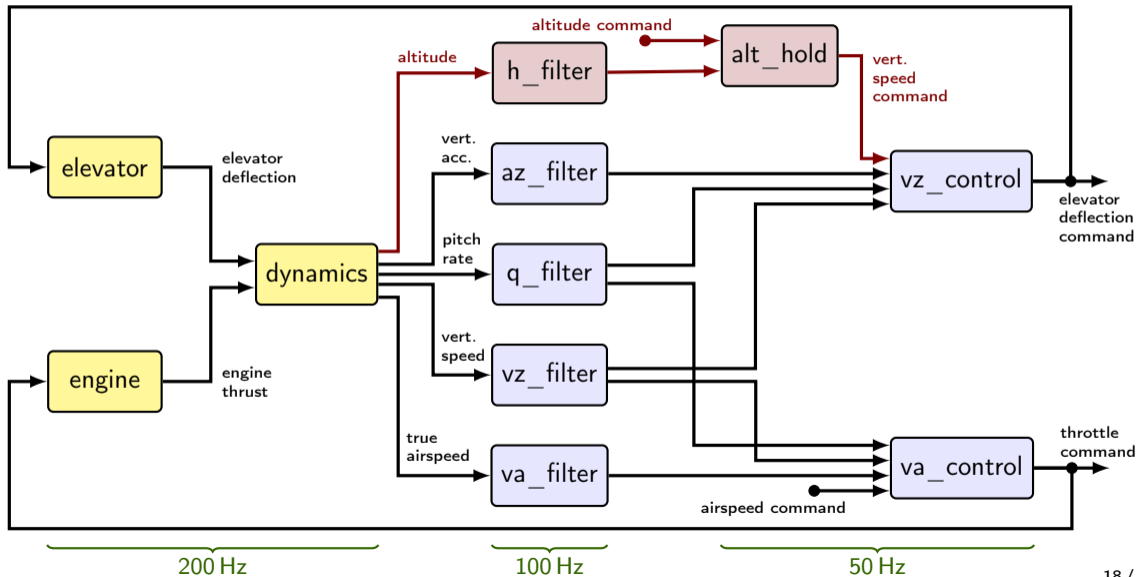
The ROSACE Case Study

[Pagetti, Saussié, Gratia, Noulard, and Siron (2014): The ROSACE Case Study: From Simulink Specification to Multi/Many-Core Execution]



The ROSACE Case Study

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The ROSACE Case Study

[Pagetti, Saussié, Gratia, Noulard, and Siron (2014): The ROSACE Case Study: From Simulink Specification to Multi/Many-Core Execution]

```
resource ops : int
node alt_hold (h_c, h_f : float) returns (vz_c : float) requires (ops = 201);
...
const H200 : rate = 1 / 2 (* base clock = 400Hz *)
const H100 : rate = 1 / 4
const H50  : rate = 1 / 8
const H10  : rate = 1 / 40

node assemblage1( h_c : float :: H10 last = 0.; (* altitude command *)
                  va_c : float :: H10 last = 0.) (* airspeed command *)
returns (d_th_c : float :: H50 last = 1.6402; (* throttle command *)
        d_e_c  : float :: H50 last = 0.0186) (* elevator deflection command *)
var h_f : float :: H100; (* altitude *)
    vz_c : float :: H50; (* vertical speed command *)
...
let
  h_f = h_filter( h when (? % 2) );
  vz_c = alt_hold( current(h_c, (? % 5)), h_f when (? % 2) );
...
resource balance ops;
latency assemblage exists <= 2
  (dynamics, h_filter, alt_hold, vz_control, elevator);
tel
```

200 Hz

100 Hz

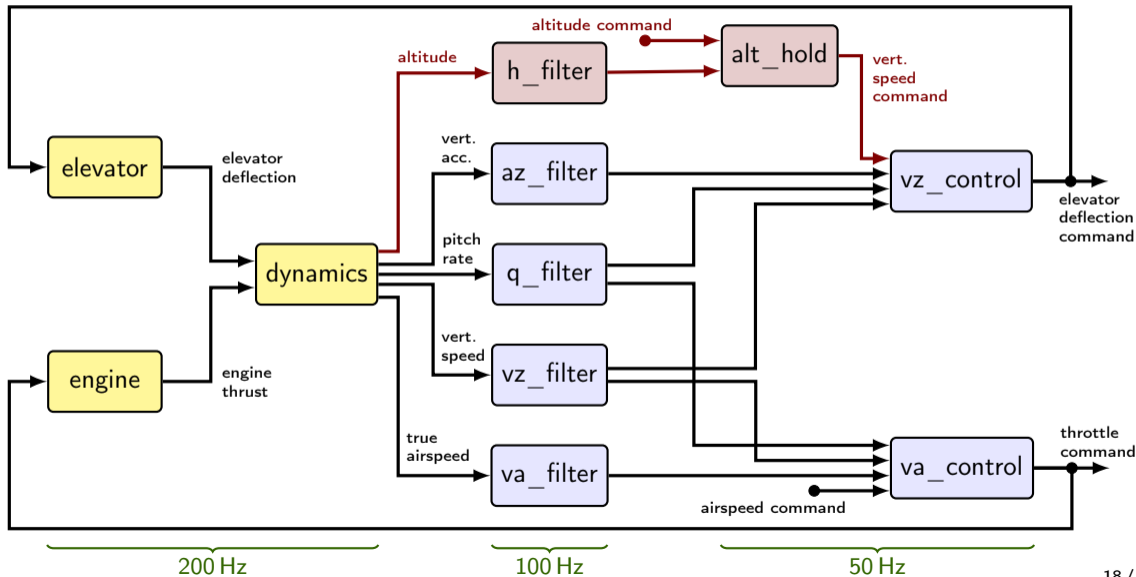
50 Hz

elevator
deflection
command

throttle
command

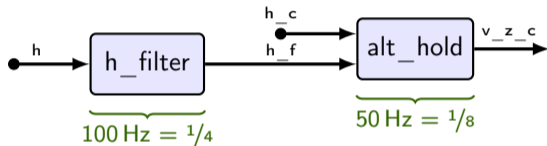
The ROSACE Case Study

[Pagetti, Saussié, Gratia, Noulard, and Siron (2014): The ROSACE Case Study: From Simulink Specification to Multi/Many-Core Execution]



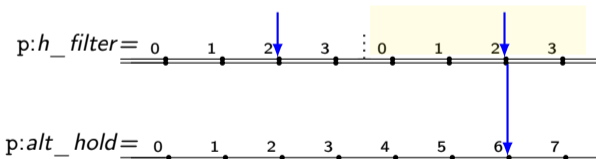
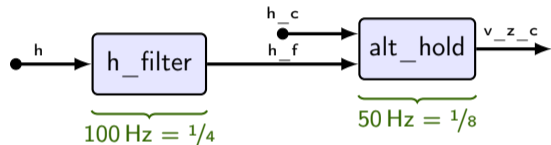
Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```



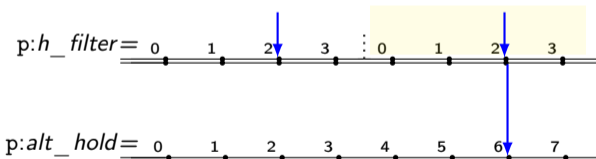
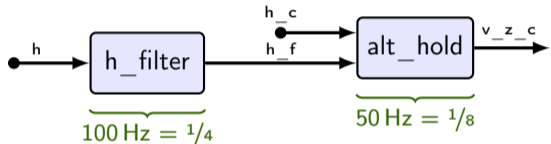
Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```



Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

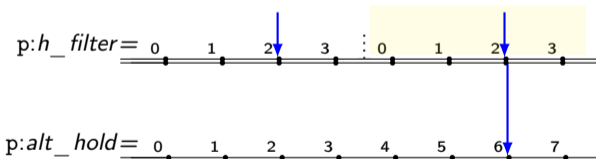
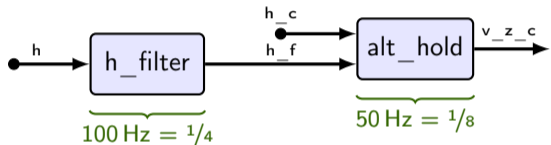
```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```



```
static int c_30 = 0;  
  
void step0()  
{  
    if (c_30 % 2 == 0) {  
        if (c_30 % 4 == 2) {  
            h_filter();    // ***  
            ...  
        }  
    } else {  
        ...  
    }  
    switch (c_30) {  
        case 2: va_control(); break;  
        case 6: alt_hold();    // ***  
                vz_control();  
                break;  
    }  
    c_30 = (c_30 + 1) % 8;  
}
```


Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```

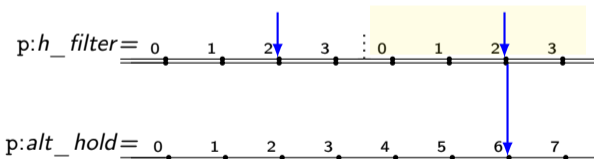
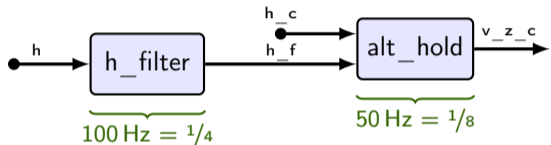


- **Source:** dataflow semantics
- **Target:** C code implicitly writing and reading static variables

```
static int c_30 = 0;  
  
void step0()  
{  
    if (c_30 % 2 == 0) {  
        if (c_30 % 4 == 2) {  
            h_filter();    // ***  
            ...  
        }  
    } else {  
        ...  
    }  
    switch (c_30) {  
        case 2: va_control(); break;  
        case 6: alt_hold();    // ***  
                vz_control();  
                break;  
    }  
    c_30 = (c_30 + 1) % 8;  
}
```

Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```

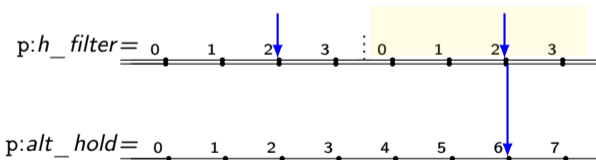
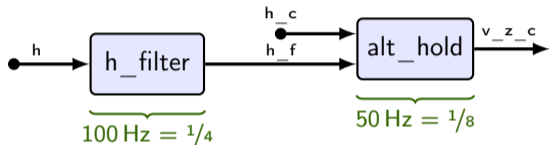


- **Source:** dataflow semantics
- **Target:** C code implicitly writing and reading static variables

```
static int c_30 = 0;  
  
void step0()  
{  
    if (c_30 % 2 == 0) {  
        if (c_30 % 4 == 2) {  
            h_filter(); // ***  
            ...  
        }  
    } else {  
        ...  
        f (concomitance)  
    }  
    switch (c_30) {  
        case 2: va_control(); break;  
        case 6: alt_hold(); // ***  
                vz_control();  
                break;  
    }  
    c_30 = (c_30 + 1) % 8;  
}
```

Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```



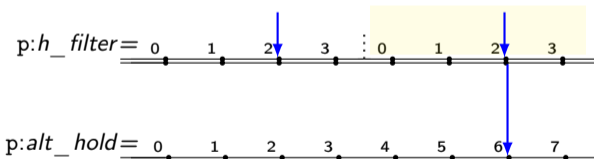
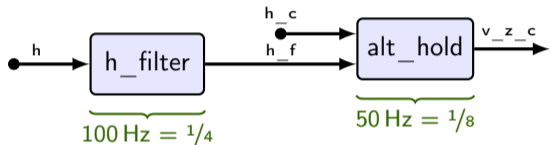
- **Source:** dataflow semantics
- **Target:** C code implicitly writing and reading static variables

```
static int c_30 = 0;  
  
void step0()  
{  
    if (c_30 % 2 == 0) {  
        if (c_30 % 4 == 2) {  
            h_filter(); // ***  
            ...  
        }  
    } else {  
        ...  
    }  
    switch (c_30) {  
    case 2: va_control(); break;  
    case 6: alt_hold(); // ***  
            vz_control();  
            break;  
    }  
    c_30 = (c_30 + 1) % 8;  
}
```

Red arrows indicate the mapping from the C code to the dataflow graph. One arrow points from the `h_filter()` call in the `if` block to the `h_filter` block in the graph. Another arrow points from the `alt_hold()` call in the `switch` block to the `alt_hold` block in the graph.

Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```



- **Source:** dataflow semantics
- **Target:** C code implicitly writing and reading static variables

```
static int c_30 = 0;
```

```
void step0()  
{
```

```
    switch (c_30) {  
        case 2: va_control(); break;  
        case 6: alt_hold();      // ***  
                vz_control();  
                break;  
    }
```

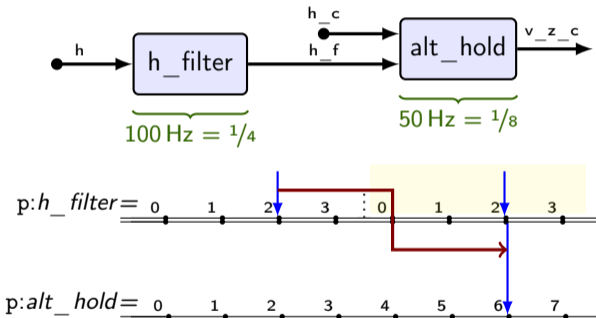
```
    if (c_30 % 2 == 0) {  
        if (c_30 % 4 == 2) {  
            h_filter(); // ***  
            ...  
        }  
    } else {
```

```
        ...  
    }  
    c_30 = (c_30 + 1) % 8;
```

```
}
```

Compilation: Model \Rightarrow Scheduling \Rightarrow Generated Code

```
h_f = h_filter(h when (? % 2));  
vz_c = alt_hold(current(h_c, (? % 5)),  
                h_f when (? % 2));
```



- **Source:** dataflow semantics
- **Target:** C code implicitly writing and reading static variables

```
static int c_30 = 0;
```

```
void step0()  
{
```

```
switch (c_30) {  
case 2: va_control(); break;  
case 6: alt_hold(); // ***  
        vz_control();  
        break;  
}
```

```
if (c_30 % 2 == 0) {  
    if (c_30 % 4 == 2) {  
        h_filter(); // ***  
        ...  
    }  
} else {
```

```
    ...  
}  
c_30 = (c_30 + 1) % 8;
```

```
}
```

```

node assemblage(h_c, va_c : float rate(100, 0))
returns (d_th_c, d_e_c : float)
var vz_c : float;
    d_e, th, h, az, va, q, vz : float;
    vz_f, va_f, h_f, az_f, q_f : float;
let
    (* 200Hz *)
    d_e = elevator(d_e_c *^ 4);
    th = engine(d_th_c *^ 4);
    (va, az, q, vz, h) = dynamics(1.6402 fby th, 0.0186 fby d_e);
    (* 100Hz *)
    h_f = h_filter(h /^ 2);
    az_f = az_filter(az /^ 2); ...
    (* 50Hz *)
    vz_c = alt_hold(h_c *^ 5, h_f /^ 2);
    d_e_c = vz_control(vz_c, vz_f /^ 2, q_f ^/ 2,
                      az_f /^ 2);
    d_th_c = va_control(va_c *^ 5, va_f /^ 2,
                       q_f /^ 2, vz_f /^ 2);

    (* dynamics -> h_filter -> alt_hold -> vz_control -> elevator <= 2 *)
    (* scheduled as real-time tasks with WCET, precedence, deadlines *)

```

```
tel
```

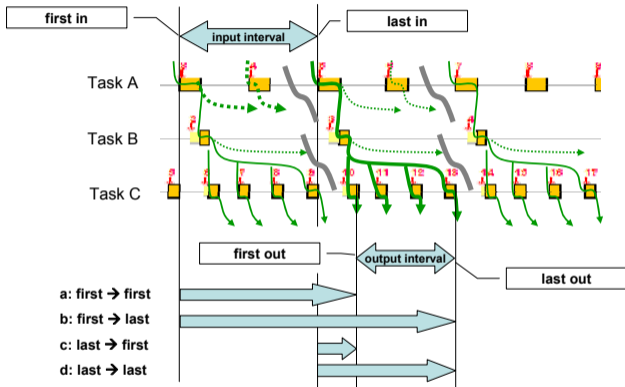
```

node assemblage(h_c, va_c : float :: 1/40 last = 0.)
returns (d_th_c, d_e_c : float :: 1/8 last = (1.6402, 0.0186))
var vz_c : float :: 1/8;
    d_e, th, h, az, va, q, vz : float :: 1/2;
    vz_f, va_f, h_f, az_f, q_f : float :: 1/4;
let
    (* 200Hz = 1/2 *)
    d_e = elevator(current(d_e_c, (? % 4)));
    th = engine(current(d_th_c, (? % 4)));
    (va, az, q, vz, h) = dynamics(th, d_e);
    (* 100Hz = 1/4 *)
    h_f = h_filter(h when (? % 2));
    az_f = az_filter(az when (? % 2)); ...
    (* 50Hz = 1/8 *)
    vz_c = alt_hold(current(h_c, (? % 5)), h_f when (? % 2));
    d_e_c = vz_control(vz_c, vz_f when (? % 2), q_f when (? % 2),
                      az_f when (? % 2));
    d_th_c = va_control(current(va_c, (? % 5)), va_f when (? % 2),
                       q_f when (? % 2), vz_f when (? % 2));

    latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
    resource balance ops;
tel

```

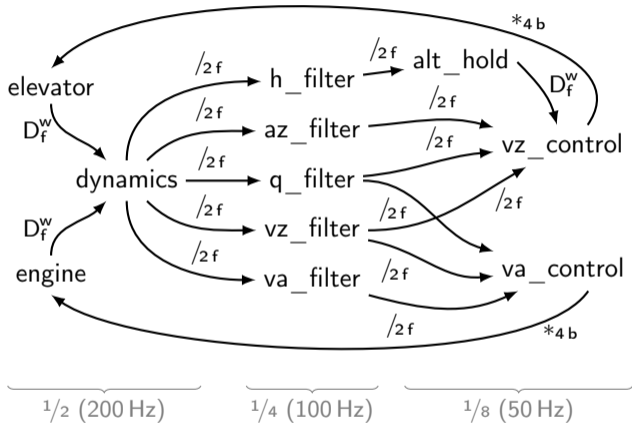
End-to-End Latency



- first-to-first = reaction time = forward
- last-to-last = data age = backward
- at least one backward path = exists
- Lots of other related work
- We ignore execution time and jitter

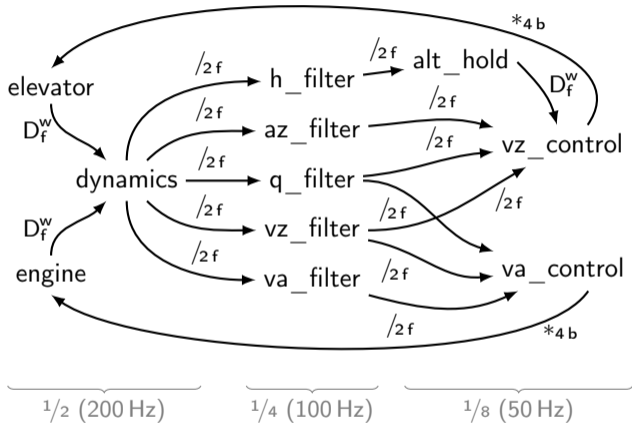
[Feiertag, Richter, Nordlander, and Jonsson (2008): A Compositional Framework for End-to-End Path Delay Calculation of Automotive Systems under Different Path Semantics]

Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
 - » concomitance (order within cycle)
- Identify and eliminate cycles
- Transform path into an ILP constraint to constrain the schedule

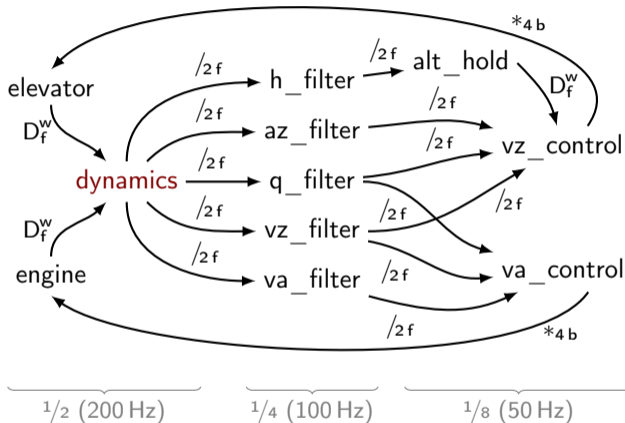
Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
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- Identify and eliminate cycles
- Transform path into an ILP constraint to constrain the schedule

```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
```

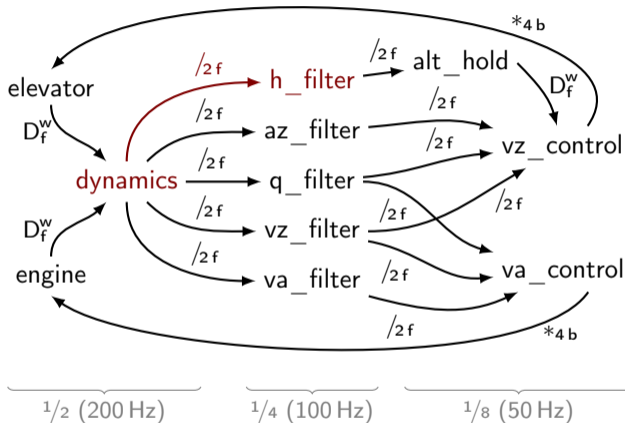
Flowgraphs and Latency chains



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```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
```

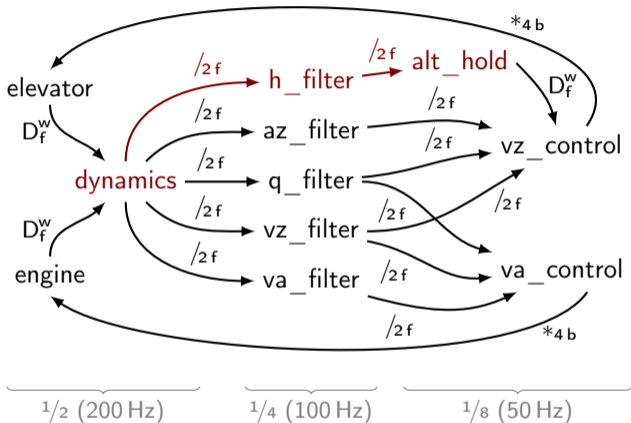
Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
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```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
```

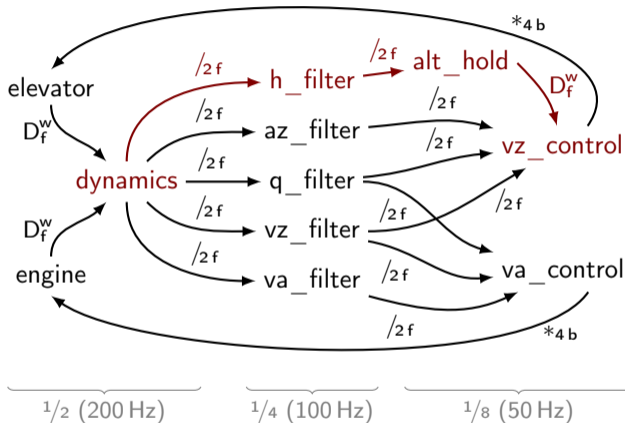
Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
 - » concomitance (order within cycle)
- Identify and eliminate cycles
- Transform path into an ILP constraint to constrain the schedule

```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
```

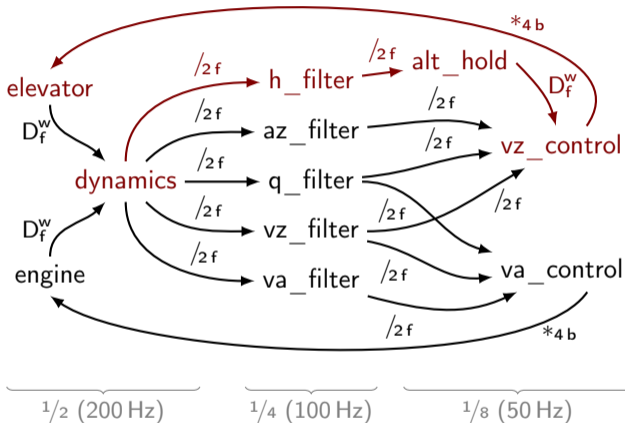
Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
 - » concomitance (order within cycle)
- Identify and eliminate cycles
- Transform path into an ILP constraint to constrain the schedule

```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
```

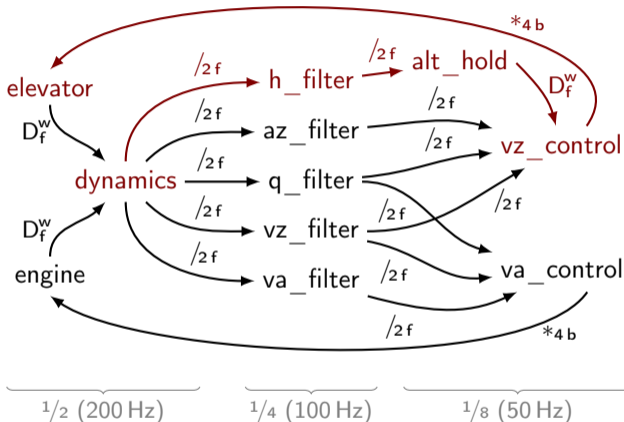
Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
 - » concomitance (order within cycle)
- Identify and eliminate cycles
- Transform path into an ILP constraint to constrain the schedule

```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
```

Flowgraphs and Latency chains



- Generate flowgraph from program, annotations:
 - » rate transitions
 - » concomitance (order within cycle)
- Identify and eliminate cycles
- Transform path into an ILP constraint to constrain the schedule

```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
latency exists <= 2 (d, h, a, v, e);
```


Flowgraph links

x	$eq_w \xrightarrow{D_f^w} eq_r$	
$\text{last } x$	$eq_w \xrightarrow{D_b^r} eq_r$	
<i>unconstrained</i>	$eq_w \xrightarrow{D_f^?} eq_r$	
$x \text{ when } (\cdot \% n)$	$eq_w \xrightarrow{/nf} eq_r$	
$(\text{last } x) \text{ when } (\cdot \% n)$	$eq_w \xrightarrow{/nb^L} eq_r$	
$\text{current}(x, (\cdot \% n))$	$eq_w \xrightarrow{*nf} eq_r$	(by default)
	$eq_w \xrightarrow{*nb} eq_r$	(if 'fast-first')
$\text{current}(\text{last } x, (\cdot \% n))$	<i>forbidden</i>	

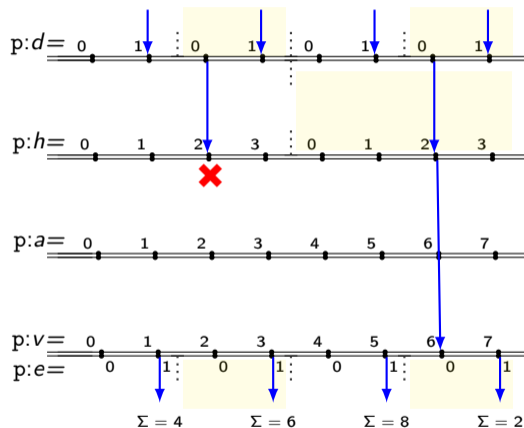
Schedule

	<i>ops</i>	<i>phase</i>	
elevator	98	1% ₂	(p:e)
engine	82	0% ₂	
dynamics	1174	1% ₂	(p:d)
h_filter	38	2% ₄	(p:h)
az_filter	37	2% ₄	
q_filter	37	2% ₄	
vz_filter	37	2% ₄	
va_filter	38	2% ₄	
alt_hold	201	6% ₈	(p:a)
vz_control	88	6% ₈	(p:v)
va_control	90	2% ₈	

- Our ROSACE implementation
 - » Cycle period = 2.5 ms (400 Hz)
 - » Allow load balancing of fastest components (200 Hz)
 - » The ops resource estimates the computations required
- Assign each component a phase relative to its period (in terms of base cycles)
- Balance ops per cycle
- Respect end-to-end latency

Schedule

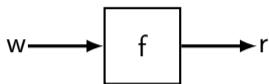
	<i>ops</i>	<i>phase</i>	
elevator	98	1%2	(p:e)
engine	82	0%2	
dynamics	1174	1%2	(p:d)
h_filter	38	2%4	(p:h)
az_filter	37	2%4	
q_filter	37	2%4	
vz_filter	37	2%4	
va_filter	38	2%4	
alt_hold	201	6%8	(p:a)
vz_control	88	6%8	(p:v)
va_control	90	2%8	



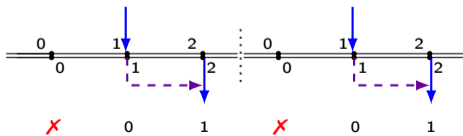
```
latency exists <= 2 (dynamics, h_filter, alt_hold, vz_control, elevator);
latency exists <= 2 (d, h, a, v, e);
```

Direct Communications

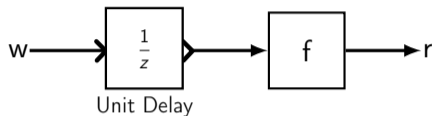
$$r = f(w)$$



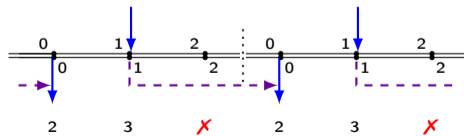
- D_f^w : Direct Write-before-read (forward concomitance)
- Dependency constraint: $p:w \leq p:r$
- $0 \leq p:r - p:w < period$



$$r = f(\text{last } w)$$

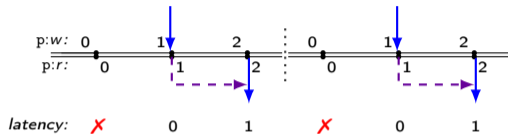


- D_b^r : Direct Read-before-write (backward concomitance)
- Dependency constraint: $p:r \leq p:w$
- $0 < p:r - p:w + period \leq period$



Minimum Pairwise Latency: same period

Direct communication: $r = w$



$r, w :: 1/3$

$p:w = 1$

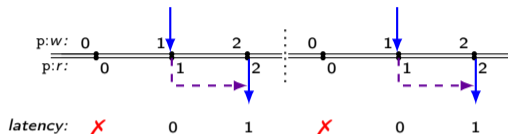
$p:r = 2$

$lat. = 1$

- $eq_w \xrightarrow{D_f^w} eq_r$
- Write-before-read: $p:w \leq p:r$
- $0 \leq p:r - p:w < period$

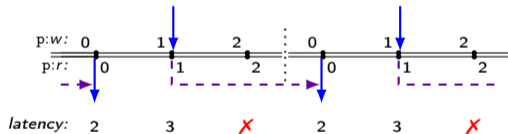
Minimum Pairwise Latency: same period

Direct communication: $r = w$



$r, w :: 1/3$
 $p:w = 1$
 $p:r = 2$
 $lat. = 1$

Delayed communication: $r = \text{last } w$

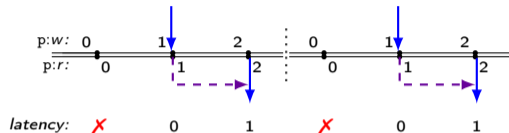


$r, w :: 1/3$
 $p:w = 1$
 $p:r = 0$
 $lat. = 2$

- $eq_w \xrightarrow{D_f^w} eq_r$
- Write-before-read: $p:w \leq p:r$
- $0 \leq p:r - p:w < period$
- $eq_w \xrightarrow{D_b^r} eq_r$
- Read-before-write: $p:r \leq p:w$
- $0 < p:r - p:w + period \leq period$

Minimum Pairwise Latency: same period

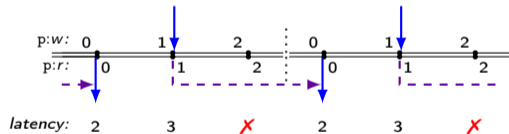
Direct communication: $r = w$



$r, w :: 1/3$
 $p:w = 1$
 $p:r = 2$
 $lat. = 1$

- $eq_w \xrightarrow{D_f^w} eq_r$
- Write-before-read: $p:w \leq p:r$
- $0 \leq p:r - p:w < period$

Delayed communication: $r = \text{last } w$



$r, w :: 1/3$
 $p:w = 1$
 $p:r = 0$
 $lat. = 2$

- $eq_w \xrightarrow{D_b^r} eq_r$
- Read-before-write: $p:r \leq p:w$
- $0 < p:r - p:w + period \leq period$

Unconstrained communication ($r = \text{last? } w$)

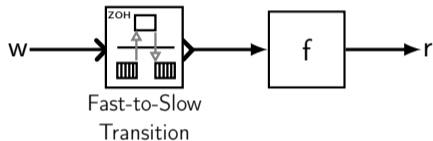
- $eq_w \xrightarrow{D_f^?} eq_r: (p:r - p:w + period(w)) \bmod period(w)$
- $eq_w \xrightarrow{D_b^?} eq_r: ((p:r - p:w + period(w) - 1) \bmod period(w)) + 1$

Rate Transitions

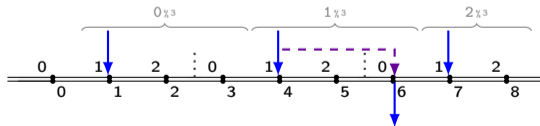
$$r = f(w \text{ when } (1 \% 3))$$

$(i \% n)$: take value i of every n

$(? \% n)$: take any of every n values

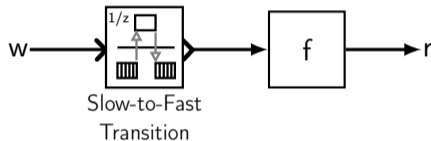


- $/_{nf}$: Fast-to-slow
(forward concomitance)

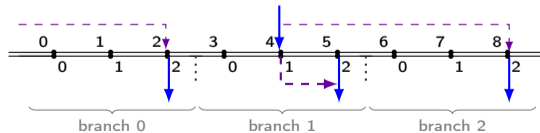


$$r = f(\text{current}(w, (1 \% 3)))$$

$(i \% n)$: i initial values, then repeat n times



- $*_{nf} \mid *_{nb}$: Slow-to-fast
(forward or backward concomitance)

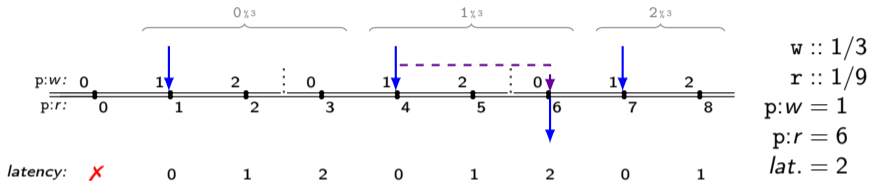


Minimum Pairwise Latency: fast-to-slow

$r = w$ when $(? \% 3)$

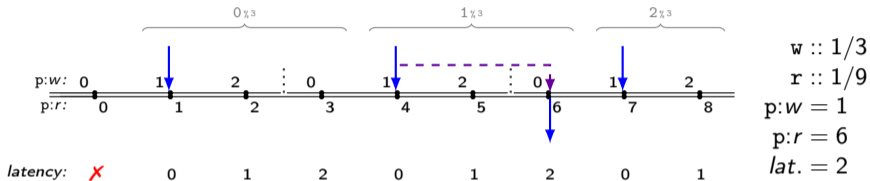
$eq_w \xrightarrow{/nf} eq_r$

$(p:r - p:w) \bmod \text{period}(w)$

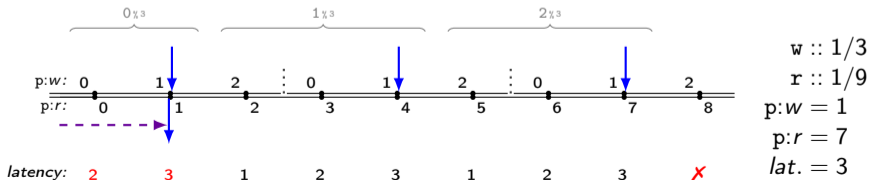


Minimum Pairwise Latency: fast-to-slow

$r = w$ when $(? \% 3)$ $eq_w \xrightarrow{/nf} eq_r$ $(p:r - p:w) \bmod \text{period}(w)$



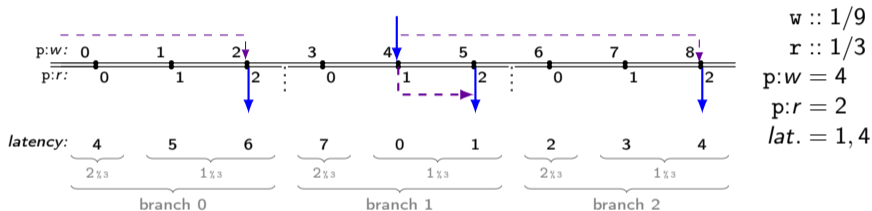
$r = (\text{last } e)$ when $(0 \% 3)$ $eq_w \xrightarrow{/nb} eq_r$
 $((\text{period}(w) + p:r - p:w - 1) \bmod \text{period}(w)) + 1$



Minimum Pairwise Latency: slow-to-fast

$$r = \text{current}(w, (1 \% 3)) \quad eq_w \xrightarrow{*nf} eq_r$$

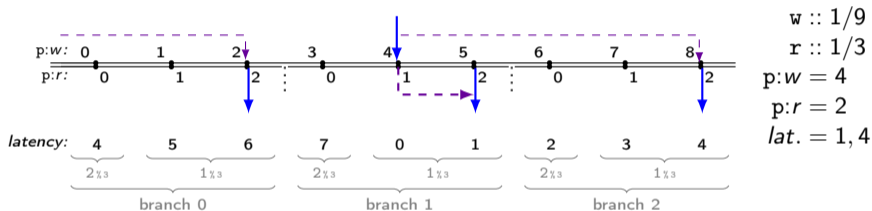
$$((branch \cdot \text{period}(r) + \text{period}(w) + p:r - p:w - 1) \bmod \text{period}(w)) + 1$$



Minimum Pairwise Latency: slow-to-fast

$$r = \text{current}(w, (1 \% 3)) \quad eq_w \xrightarrow{*nf} eq_r$$

$$((branch \cdot \text{period}(r) + \text{period}(w) + p:r - p:w - 1) \bmod \text{period}(w)) + 1$$



$$r = \text{current}(\text{last } w, (? \% 3))?$$

- Not allowed. Not enough 'memories'.
- Must be normalized to

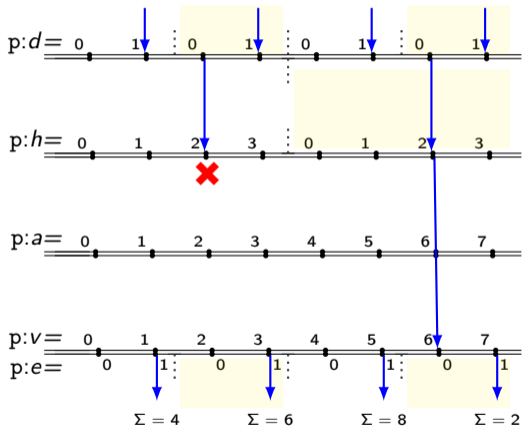

```

r = current(t, (? % 3));
t = last w;
            
```

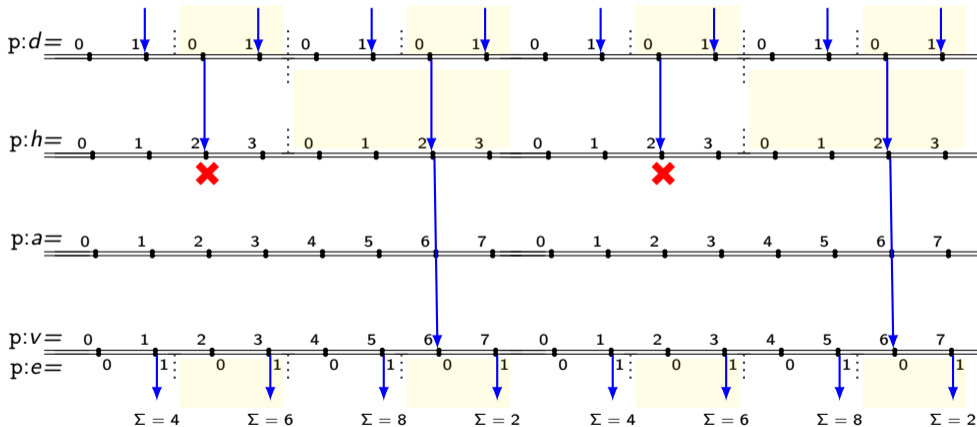
End-to-End Latency: the wrong way

- Define pairwise latencies for each link type.
- Chain them together into a sequence.
- Difficult to handle branching and dead ends.
- Difficult to explain.
- Complicated formulas.
- There's a better way. . .

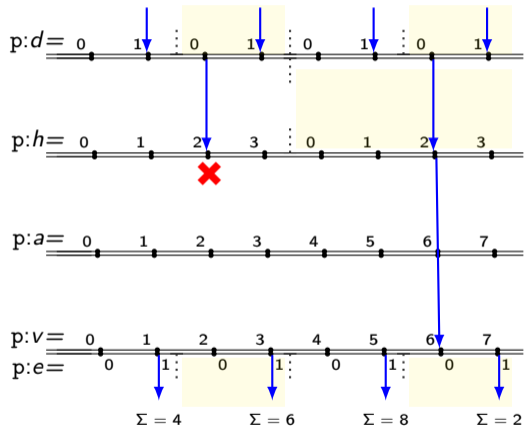
Constraining End-to-end Latency



Constraining End-to-end Latency

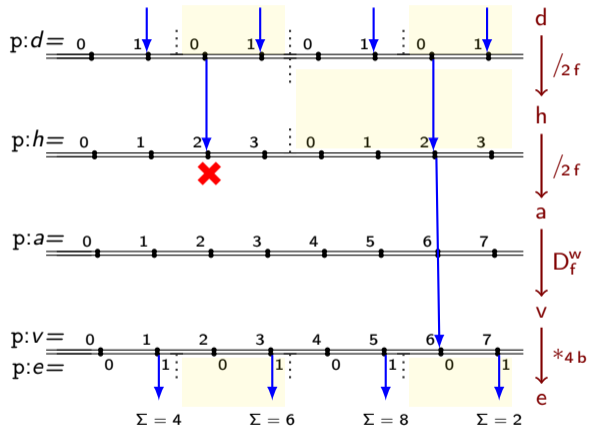


Constraining End-to-end Latency



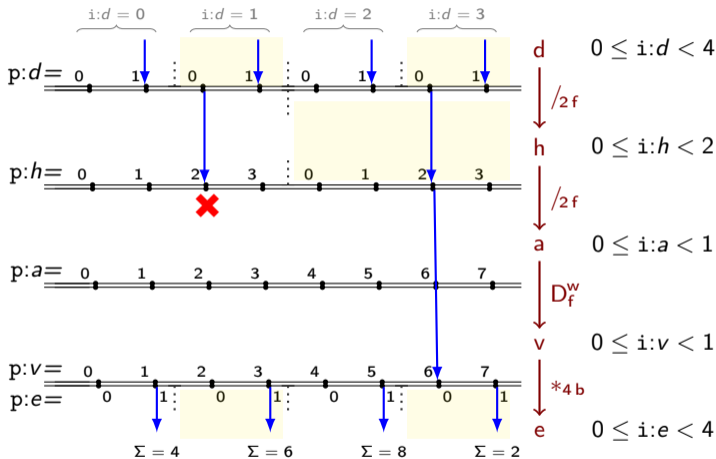
(View online at <https://www.tbrk.org/dataflow/showlatency>)

Constraining End-to-end Latency



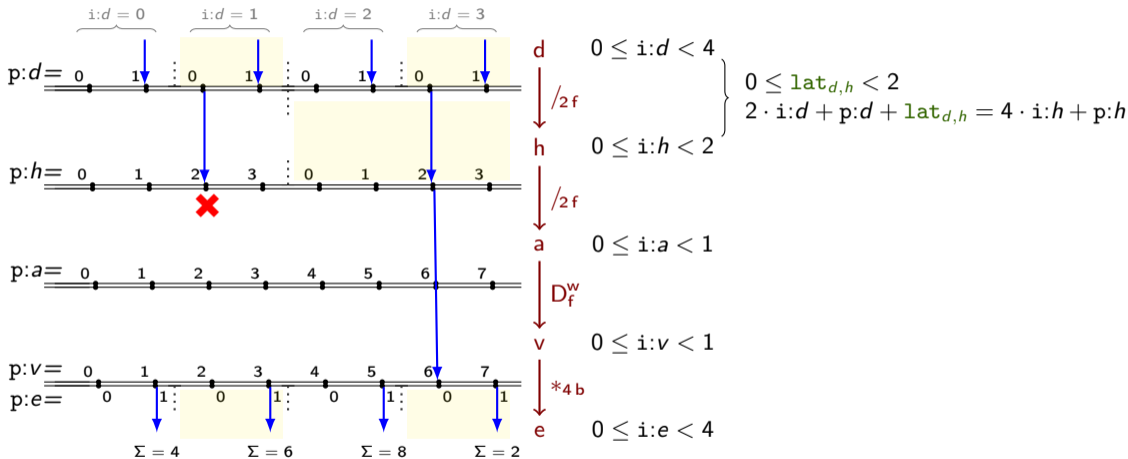
(View online at <https://www.tbrk.org/dataflow/showlatency>)

Constraining End-to-end Latency

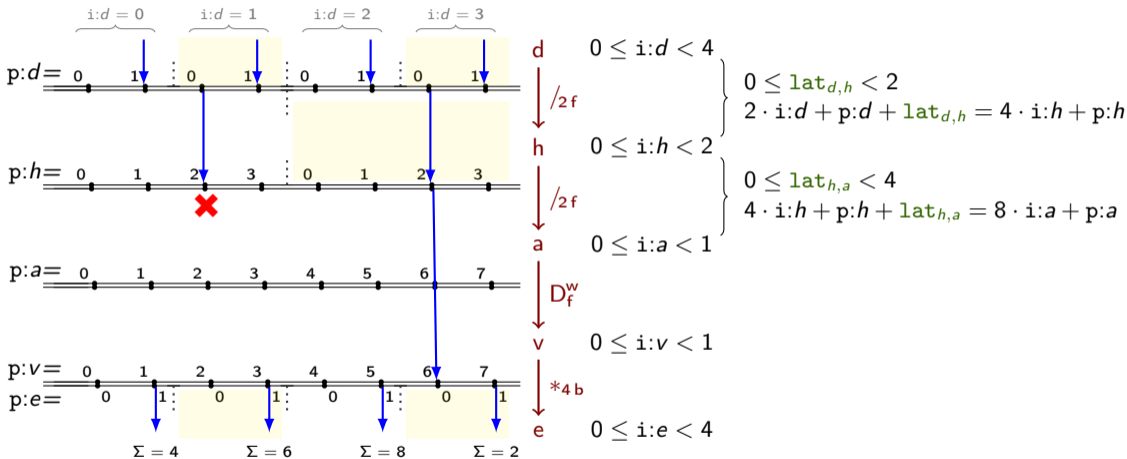


(View online at <https://www.tbrk.org/dataflow/showlatency>)

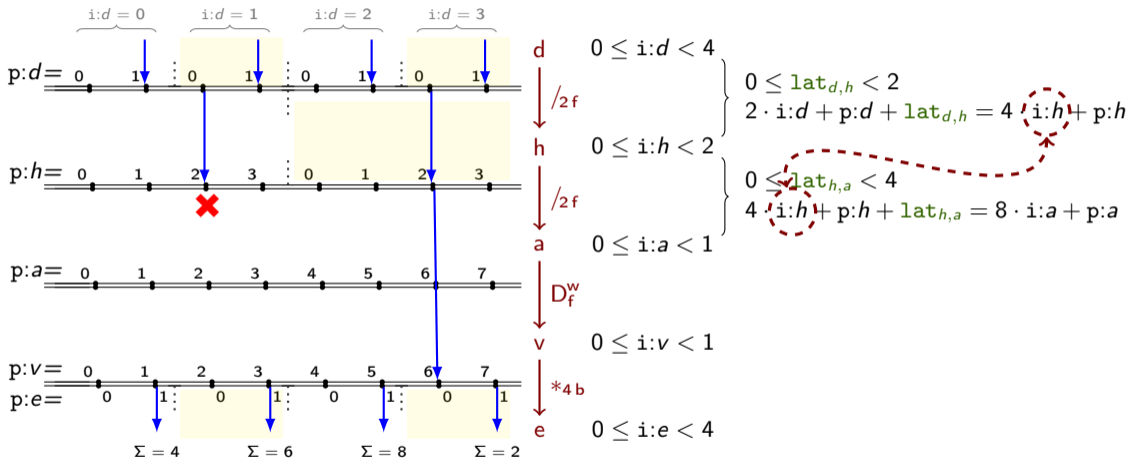
Constraining End-to-end Latency



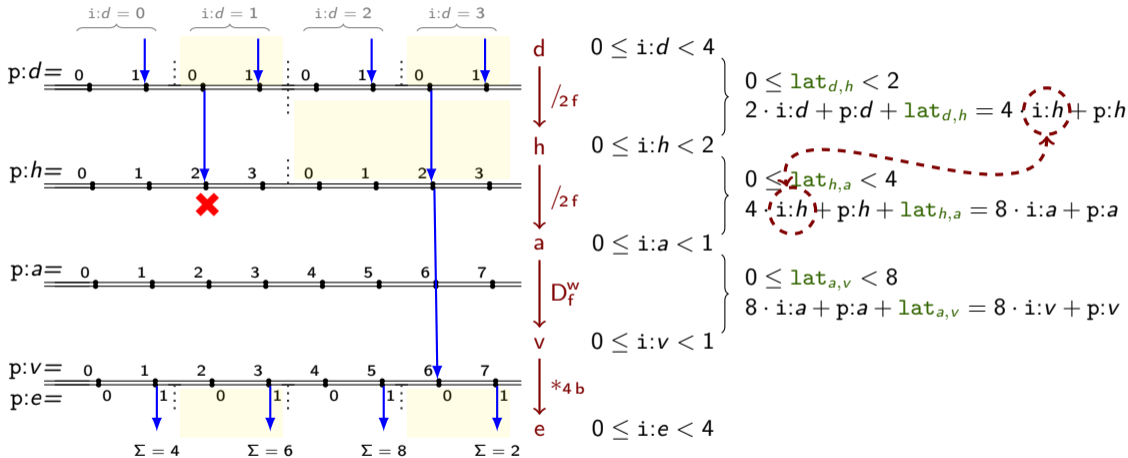
Constraining End-to-end Latency



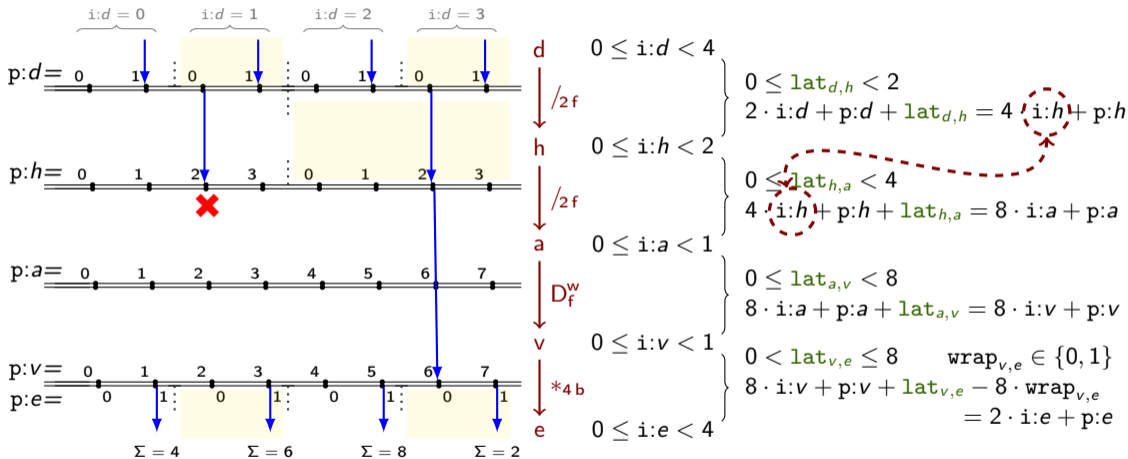
Constraining End-to-end Latency



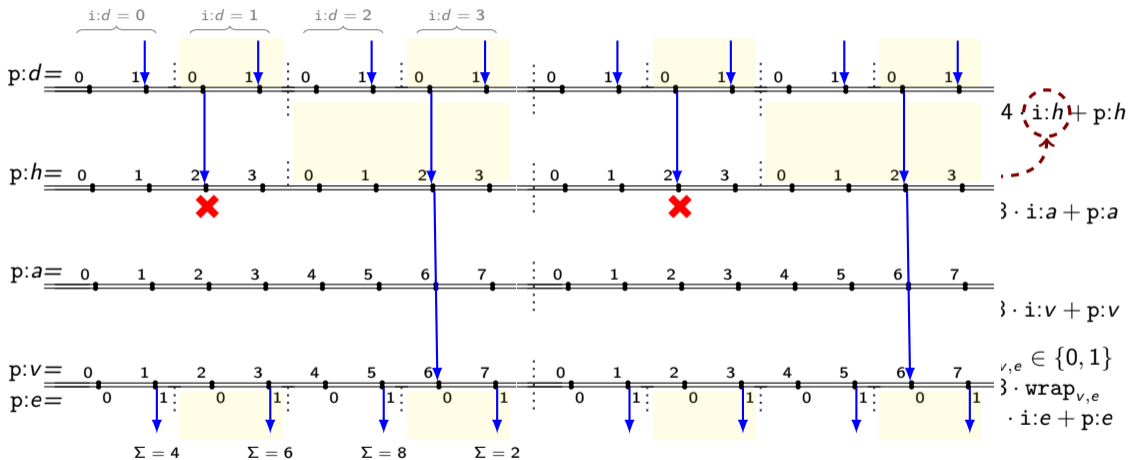
Constraining End-to-end Latency



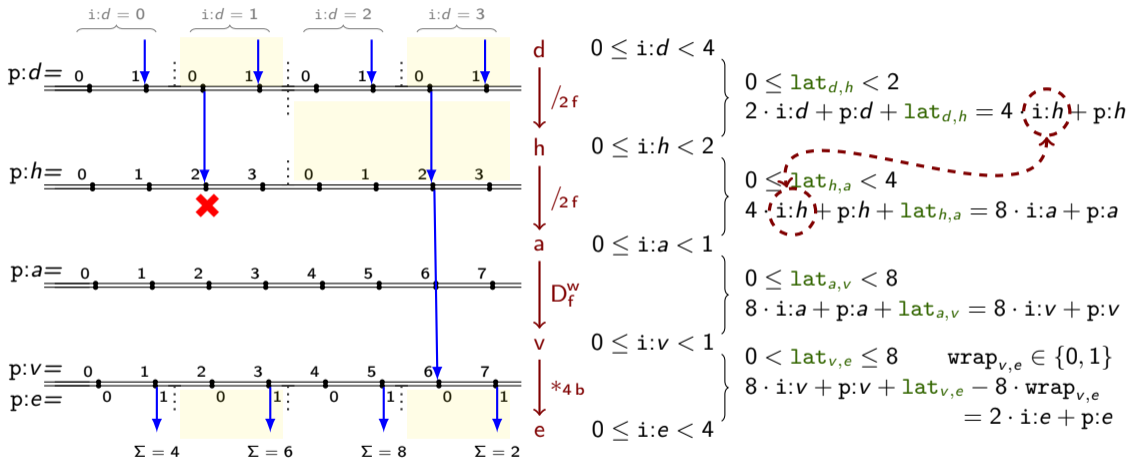
Constraining End-to-end Latency



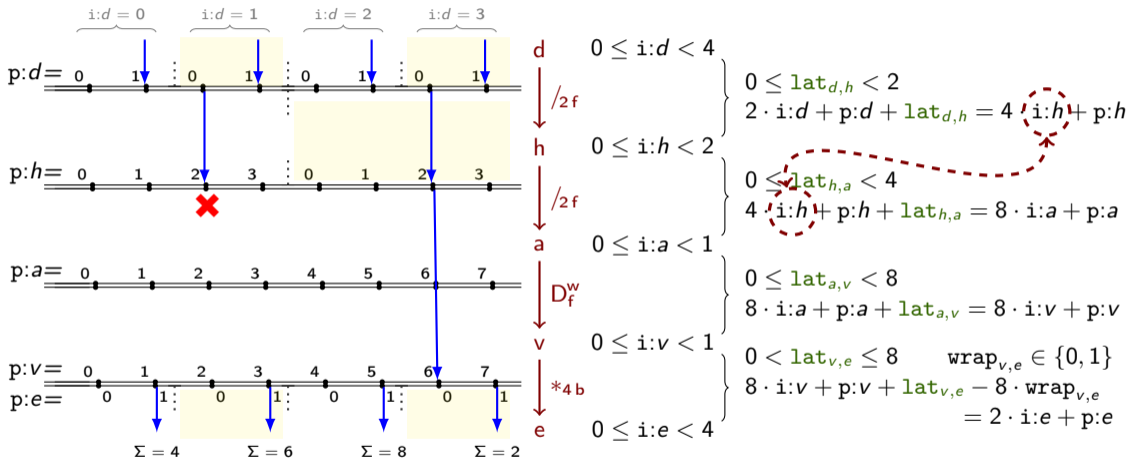
Constraining End-to-end Latency



Constraining End-to-end Latency



Constraining End-to-end Latency



$$\text{lat}_{d,h} + \text{lat}_{h,a} + \text{lat}_{a,v} + \text{lat}_{v,e} \leq 2$$

Chains of constraints

latency forward/backward $\leq B (\dots, w, r, \dots)$

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For each link $w \xrightarrow{s,c} r$,

Chains of constraints

latency forward/backward $\leq B (\dots, w, r, \dots)$

For each link $w \xrightarrow{s,c} r$,

$$0 \leq i:r < hp/\text{period}(r)$$

$$\begin{array}{l} 0 \leq \text{lat}_{w,r} < L \quad \text{for } c = f \\ 0 < \text{lat}_{w,r} \leq L \quad \text{for } c = b \end{array} \quad \left\{ \begin{array}{l} \text{where } L = \text{period}(r) \text{ if forward} \\ \text{and } L = \text{period}(w) \text{ if backward} \end{array} \right.$$

$$0 \leq \text{wrap}_{w,r} \leq 1 \quad \begin{array}{l} \text{if forward and } s \notin \{D^w, *_n\} \\ \text{or if backward and } s \notin \{D^w, /_n\} \end{array}$$

$$\text{period}(w) \cdot i:w + p:w + \text{lat}_{w,r} - hp \cdot \text{wrap}_{w,r} = \text{period}(r) \cdot i:r + p:r.$$

- Each intermediate instance is both a reader and a writer, and thus constrained by two equations.
- forward: attach chains from the top
- backward: attach chains to the bottom

Before scheduling

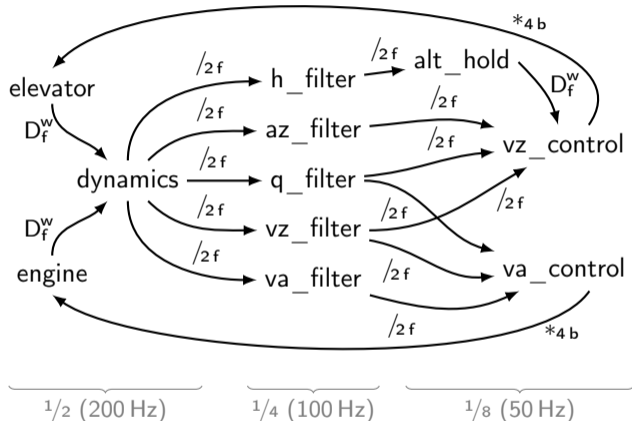
1. Construct flow graph from program
2. Remove potential cycles by flipping the microcausality
3. Use to generate ILP constraints (causality, end-to-end latency)

After scheduling: convert to dependency graph

1. Drop edges between equations that cannot execute in any phase.
2. Flip the cobackward (b) edges.
3. Use with standard algorithm to schedule equations within a step function.

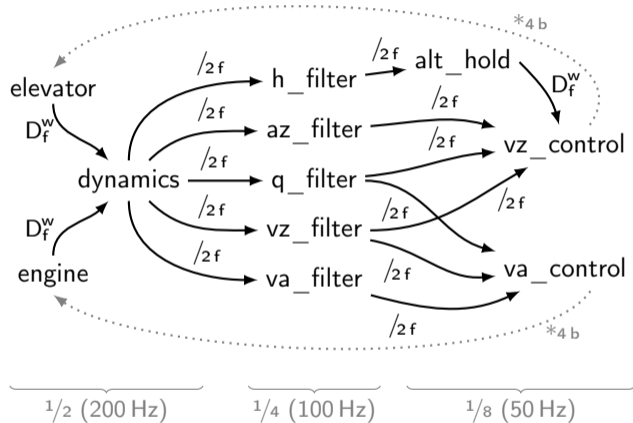
ROSACE example: flow graph \rightarrow dependency graph

	<i>ops</i>	<i>phase</i>
elevator	98	1%2
engine	82	0%2
dynamics	1174	1%2
h_filter	38	2%4
az_filter	37	2%4
q_filter	37	2%4
vz_filter	37	2%4
va_filter	38	2%4
alt_hold	201	6%8
vz_control	88	6%8
va_control	90	2%8



ROSACE example: flow graph \rightarrow dependency graph

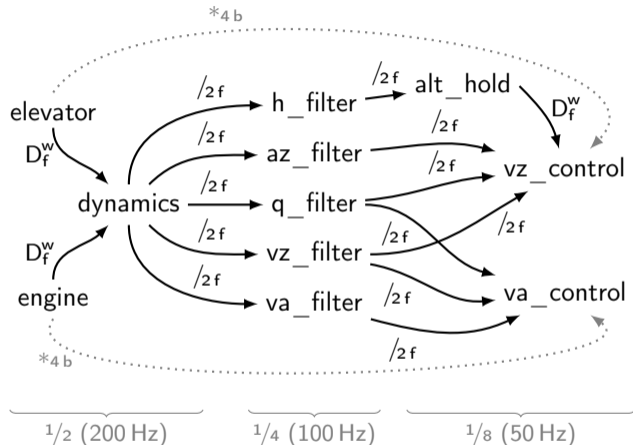
	<i>ops</i>	<i>phase</i>
elevator	98	1%2
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h_filter	38	2%4
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va_filter	38	2%4
alt_hold	201	6%8
vz_control	88	6%8
va_control	90	2%8



- Remove all edges between equations that can never execute in the same phase.
- Reverse edges whose microcausality is b .

ROSACE example: flow graph \rightarrow dependency graph

	<i>ops</i>	<i>phase</i>
elevator	98	1%2
engine	82	0%2
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alt_hold	201	6%8
vz_control	88	6%8
va_control	90	2%8



- Remove all edges between equations that can never execute in the same phase.
- Reverse edges whose microcausality is b .

ROSACE example: generated code

```
static int c = 0;
static float h_c = 0, d_th_c = 1.6402, d_e_c = 0.0186, ...;
static float vz_c, ..., q_f;

void step0()
{
    if (c % 2 == 0) {
        engine();
        if (c % 4 == 2) {
            vz_filter(); h_filter(); va_filter(); q_filter(); az_filter();
        }
    } else {
        elevator(); dynamics();
    }
    switch (c) {
        case 2: va_control(); break;
        case 6: alt_hold(); vz_control(); break;
    }
    c = (c + 1) % 8;
}
```

Generalize the clock-directed scheme [Biernacki, Colaço, Hamon, and Pouzet (2008): Clock-directed modular code generation for synchronous data-flow languages]

- `--compile n` generates n step functions
 - » For the i th step function, $step_i$, `List .filter_map` equations by phase offset.
 - » Generate dependency graph ignoring variables not in $step_i$
—macro-scheduling guarantees they will already have been calculated.
 - » Micro-schedule equations in $step_i$ w.r.t. dependencies and phase offset/rate.
- Generate multiple `Obc` step methods, buffer values in state variables.
- Optimize the `Obc` by joining adjacent `case` statements.

Specialized case construct

```
case (state(c_3) mod 3) {  
  0: { skip }  
  1: { state(s2) := filter(state(s1)) }  
  2: { skip }  
  else undefined  
};  
case (state(c_3) mod 3) {  
  0: { state(s1) := filter(s0) }  
  1: { skip }  
  2: { skip }  
  else undefined  
};
```



```
case (state(c_3) mod 3) {  
  0: { state(s1) := filter(s0) }  
  1: { state(s2) := filter(state(s1)) }  
  2: { skip }  
  else undefined  
};
```

The 'else undefined' simplifies optimisation under (implicit) invariants

```
case (state(c_3) mod 24) {  
  7: { state(x) := read_real() }  
  23: { y := read_real() }  
  else undefined }
```



```
if (state(c_3) mod 24 = 7) {  
  state(x) := read_real()  
} else {  
  y := read_real()  
}
```

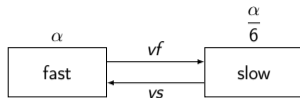
```
case (state(c_3) mod 24) {  
  7: { state(x) := read_real() }  
  15: { skip }  
  23: { y := read_real() }  
  else undefined }
```



```
case (state(c_3) mod 24) {  
  7: { state(x) := read_real() }  
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  else undefined }
```

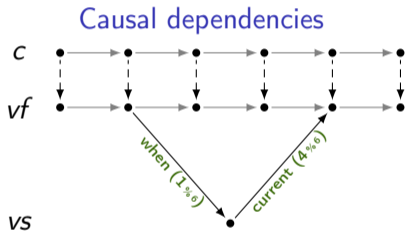
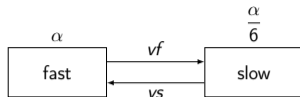
Causality, Scheduling, and Semantics

```
c = last c + 1;           -- last c = -1
vf = current(vs, (4 % 6)) + c;
vs = vf when (1 % 6) + 5; -- last vs = 0
```



Causality, Scheduling, and Semantics

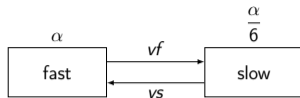
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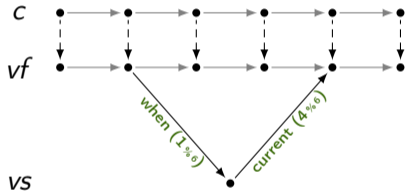
Causality, Scheduling, and Semantics

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vf = current(vs, (4 % 6)) + c;
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```



Causal dependencies

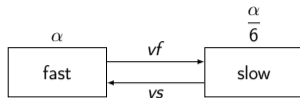


<i>vf</i>	0	1	2	3	10	11	12	13	14	15	28	29	...
<i>c</i>	0	1	2	3	4	5	6	7	8	9	10	11	...
<i>vs</i>	6						18						...

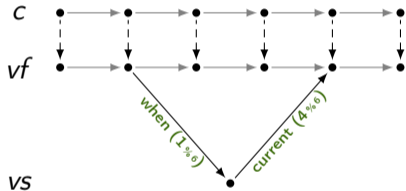
Causality, Scheduling, and Semantics

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Causal dependencies

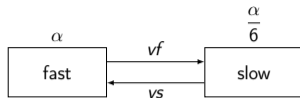


vf	0	1	2	3	10	11	12	13	14	15	28	29	...
c	0	1	2	3	4	5	6	7	8	9	10	11	...
vs					6						18		...

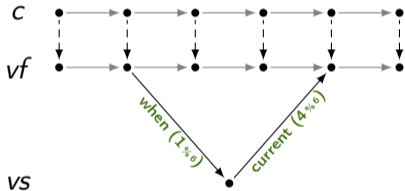
Causality, Scheduling, and Semantics

```

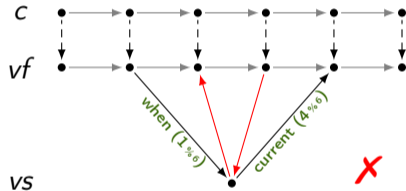
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```



Causal dependencies



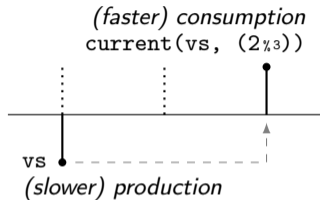
Scheduling dependencies



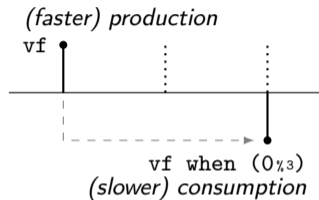
vf	0	1	2	3	10	11	12	13	14	15	28	29	...
c	0	1	2	3	4	5	6	7	8	9	10	11	...
vs					6						18		...

Adding equations to relax constraints/add buffering

Hold slow around fast reads

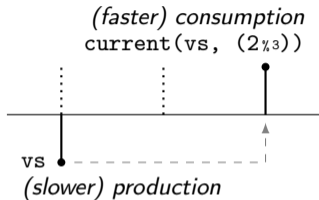


Hold fast around fast writes

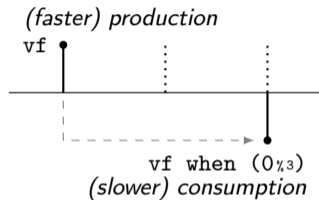


Adding equations to relax constraints/add buffering

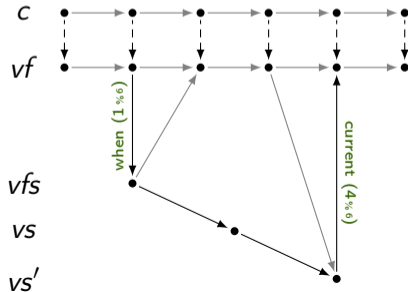
Hold slow around fast reads



Hold fast around fast writes



```
c = 0 fby (c + 1);  
vf = current(vs', (4 % 6)) + c;  
vfs = vf when (1 % 6)  
vs = vfs + 5;  
vs' = vs
```



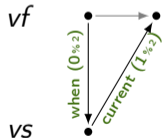
Causality: 1

- Which programs are valid? I.e., which have a semantics?
- Consider causality across the least common multiple of periods.
- Implicit dependencies to past elements on same flow.

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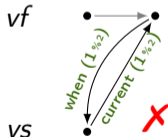
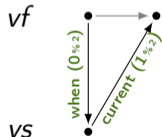
```
vf = current(vs, (1%2));  
vs = vf when (0%2) + 1;
```



Causality: 1

- Which programs are valid? I.e., which have a semantics?
- Consider causality across the least common multiple of periods.
- Implicit dependencies to past elements on same flow.

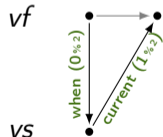
```
vf = current(vs, (1%2));   vf = current(vs, (1%2));  
vs = vf when (0%2) + 1;   vs = vf when (1%2) + 1;
```



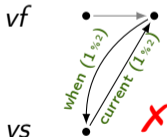
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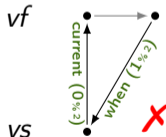
$vf = \text{current}(vs, (1\%2));$
 $vs = vf \text{ when } (0\%2) + 1;$



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 $vs = vf \text{ when } (1\%2) + 1;$



$vf = \text{current}(vs, (0\%2));$
 $vs = vf \text{ when } (1\%2) + 1;$



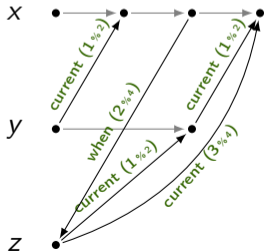
Causality: 2

Causality relations between $x :: \alpha$, $y :: \frac{\alpha}{2}$, and $z :: \frac{\alpha}{4}$.

```
x = current(y, (1 % 2))  
    + current(z, (3 % 4)) + 2;
```

```
y = current(z, (1 % 2)) + 20;
```

```
z = x when (2 % 4) + 200;
```



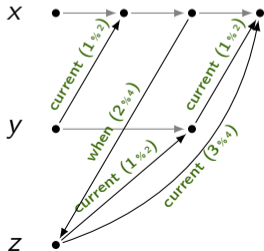
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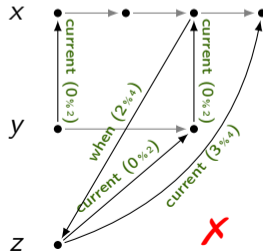
```
z = x when (2 % 4) + 200;
```



```
x = current(y, (0 % 2))  
  + current(z, (3 % 4)) + 2;
```

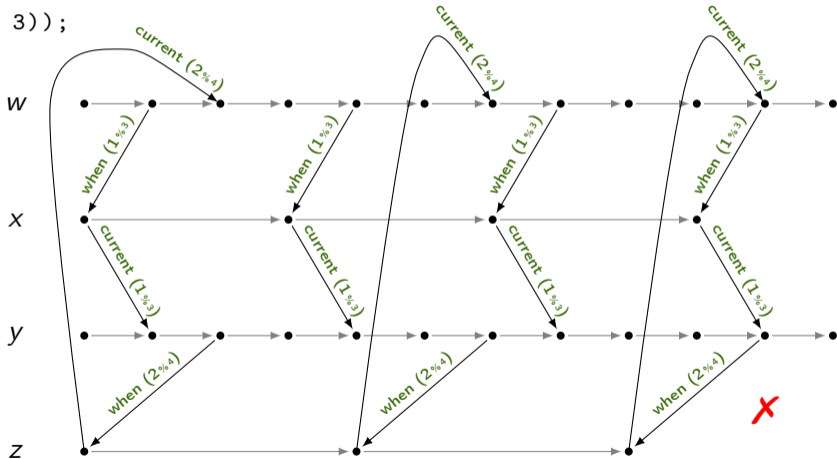
```
y = current(z, (1 % 2)) + 20;
```

```
z = x when (2 % 4) + 200;
```



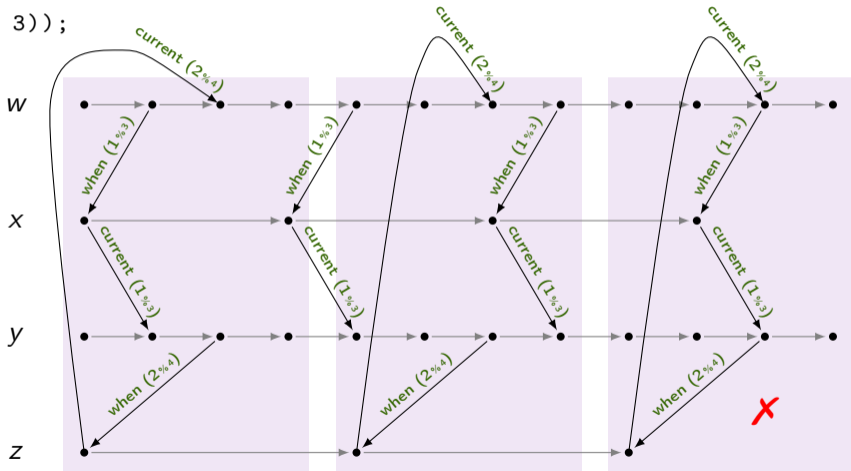
Causality: non-harmonic rates with 'shifting'

```
w = current(z, (2 % 4));  
x = w when (1 % 3);  
y = current(x, (1 % 3));  
z = y when (2 % 4);
```



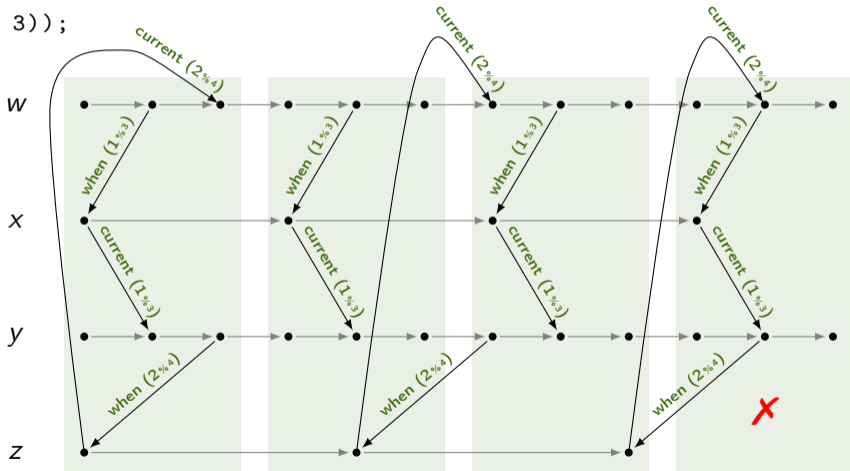
Causality: non-harmonic rates with 'shifting'

```
w = current(z, (2 % 4));  
x = w when (1 % 3);  
y = current(x, (1 % 3));  
z = y when (2 % 4);
```



Causality: non-harmonic rates with 'shifting'

```
w = current(z, (2 % 4));  
x = w when (1 % 3);  
y = current(x, (1 % 3));  
z = y when (2 % 4);
```



Related Work: Lucy-n

- Model [Cohen, Duranton, Eisenbeis, Pagetti, Plateau, and Pouzet (2006): N-Synchronous Kahn networks: a relaxed model of synchrony for real-time systems] and language [Mandel, Plateau, and Pouzet (2010): Lucy-n: a n-Synchronous extension of Lustre]
- Flexible scheduling patterns (0010(010)) and buffering
- Notion of jitter with clock envelopes [Cohen, Mandel, Plateau, and Pouzet (2008): Abstraction of Clocks in Synchronous Data-flow Systems]
- Sophisticated type-based analysis for causality and buffer sizes
- Less focus on code generation

Our work

- Less flexible scheduling
- Buffering is implicit and limited to size ≤ 1
- Less clock typing, more causality
- Generate imperative code

Related Work: looss et al.

- “1-synchronous” programs [looss, Pouzet, Cohen, Potop-Butucaru, Souyris, Bregeon, and Baufreton (2020): 1-Synchronous Programming of Large Scale, Multi-Periodic Real-Time Applications with Functional Degrees of Freedom]
- Two-element clocks: [*phase, period*]
($0^k 10^{n-k-1}$ or $0^k (10^{n-1})$, where n is the period and $0 \leq k < n$ is the phase)
- Related to work on affine clocks
 - » [Curic (2005): Implementing Lustre Programs on Distributed Platforms]
[with Real-Time Constraints
 - » [Smarandache, Gautier, and Le Guernic (1999): Validation of Mixed Signal-Alpha]
[Real-Time Systems through Affine Calculus on Clock Synchronisation Constraints]
- Several operators: **when**, **current**, delay, delayfby, buffer, bufferfby
- Prototype in Heptagon: introduces (lots of) whens and merges

Our work

- Simpler clocks, fewer operators, implicit buffering
- Generate imperative code directly

- Programming language for composing tasks
 - » Particularity: tasks must terminate in one cycle
 - » Semantics, static analysis (clock types), compilation
- Use an ILP solver for scheduling
 - » Load balancing
 - » End-to-end latency
- Prototype compiler in OCaml with ILP scheduling and basic code generation
- Tested on Airbus example with 5000 nodes (compiles in approx. 45 minutes).

M2 internship P. Robert

- Clock inference
- Inlining
- Normalization
- Introduction of 'buffers' by inserting assignments.

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