Plan

Synchronous Circuit
- Combinational Circuit
- Sequential Circuit
- Digital Watch

Binary Algebra
- Boolean Algebra
- Binary z^- Transform
- 2-adic Numbers

Electronic Circuit
- Transistor
- Silicon Process
- MOS Structures

Silicon Arithmetic
- Counters
- Adders
- Multipliers

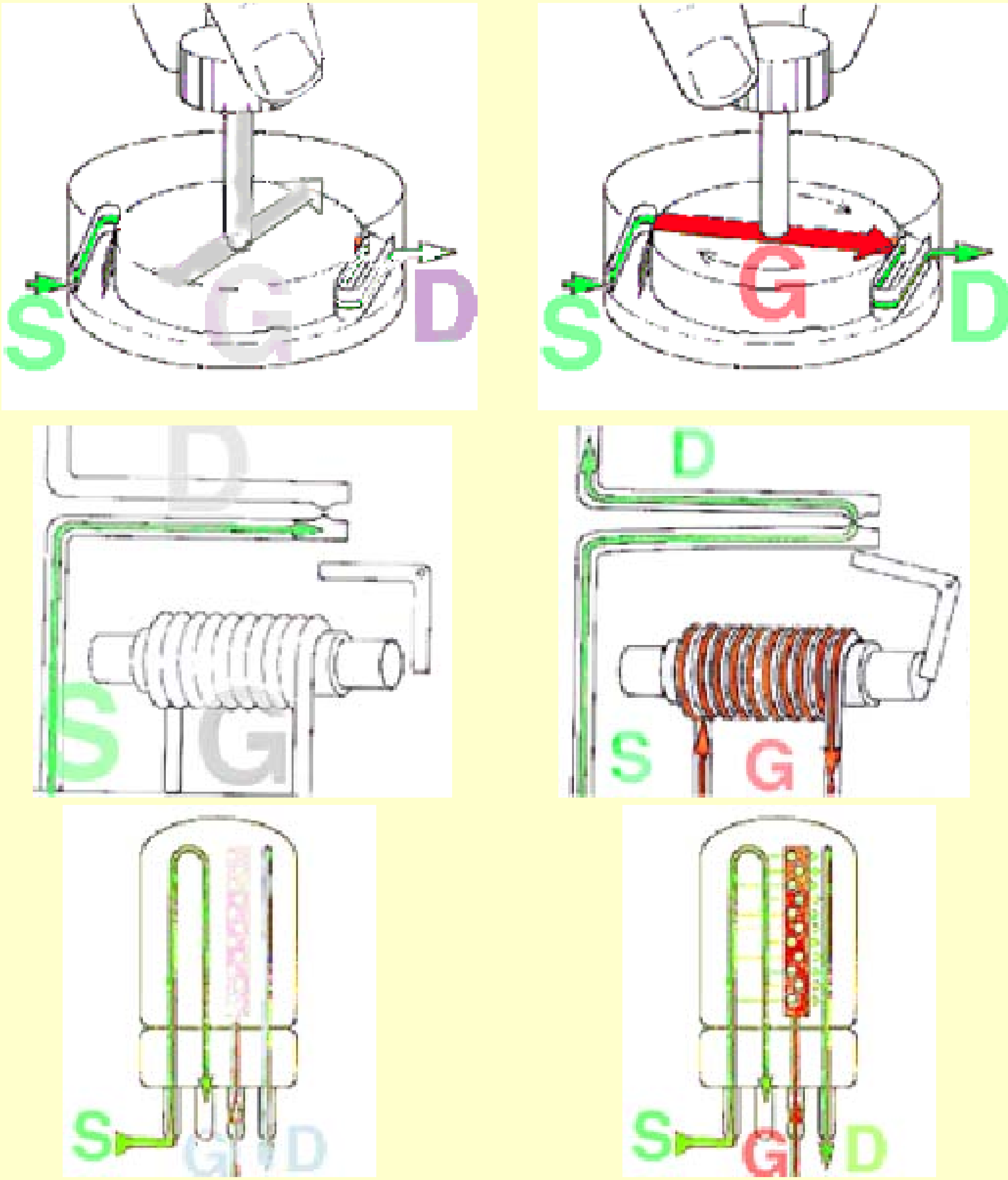
Universal Machines
- Microprocessor
- Programmable Logic
- Computable Functions

Digital Physics
- CCD Camera
- Radiation Detector
- Heat Equation

Information Theory
- Shannon's Theory
- Entropy Coding
- Error Coding

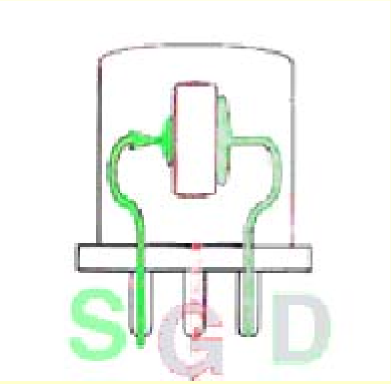
Audio & Video
- Digital Audio
- JPEG Compression
- Half Toning

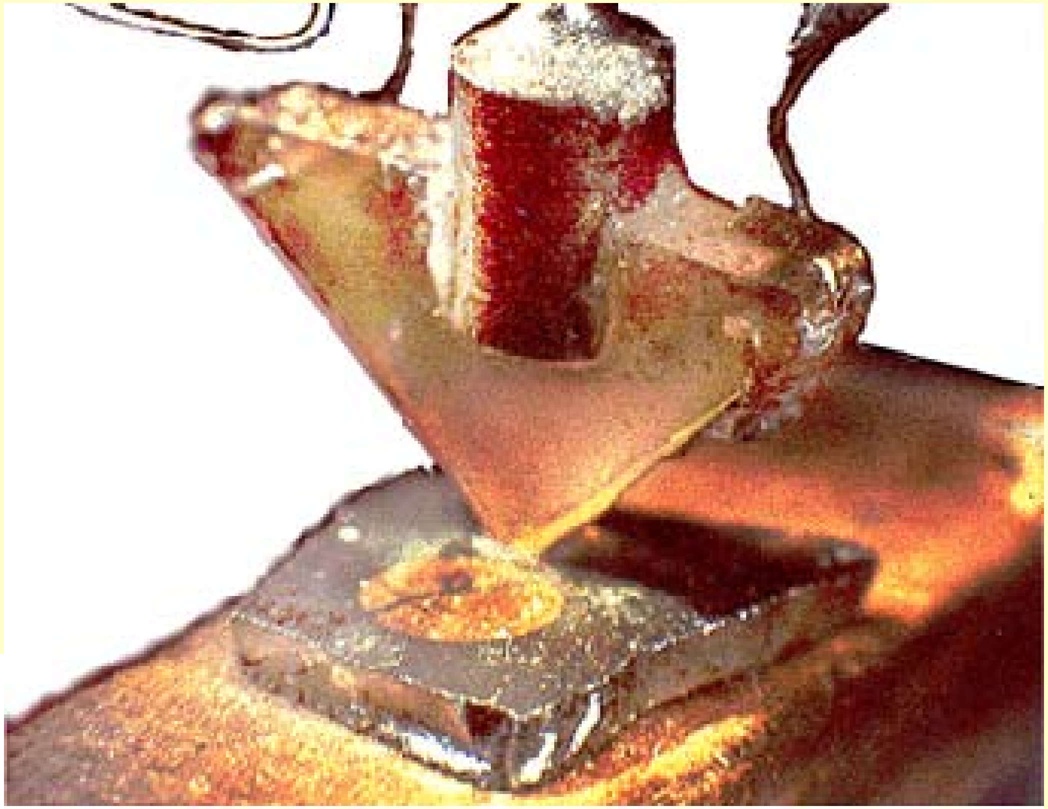
Switch

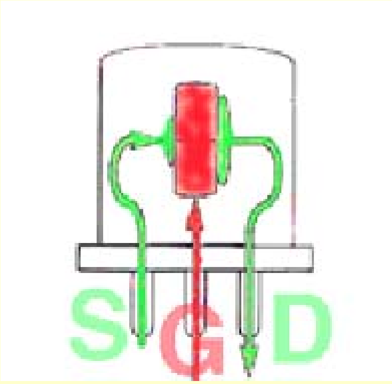

S
G
D
S
G
D
D
S
G
D
S
G
S
G
D
S
G
D


Mémoire d'ordinateur, 195*
Mémoire 16Kb
Tores de ferrite
puce dRAM
64Mb, 199*
Electronique
de contrôle :
lampes à vide

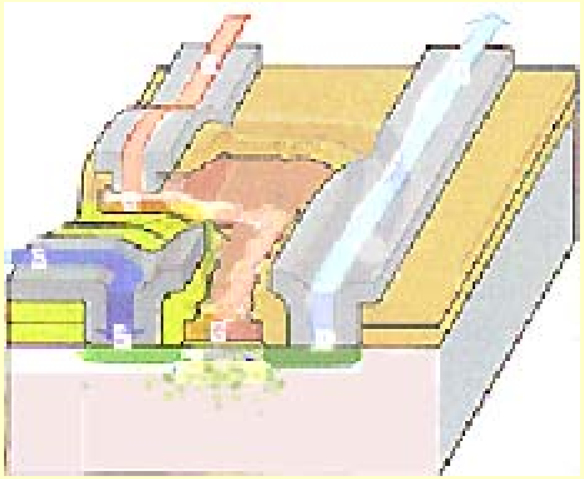
Transistor

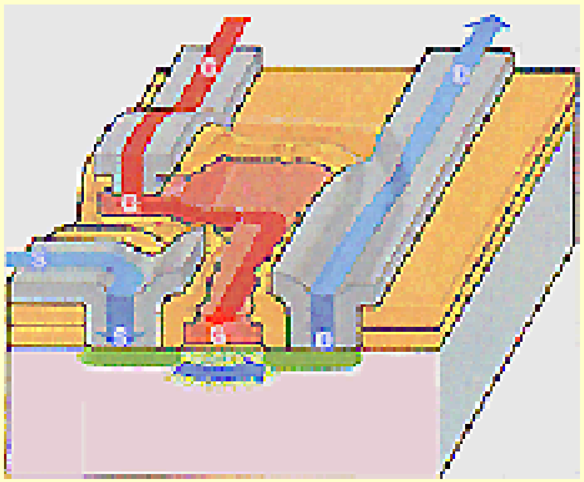


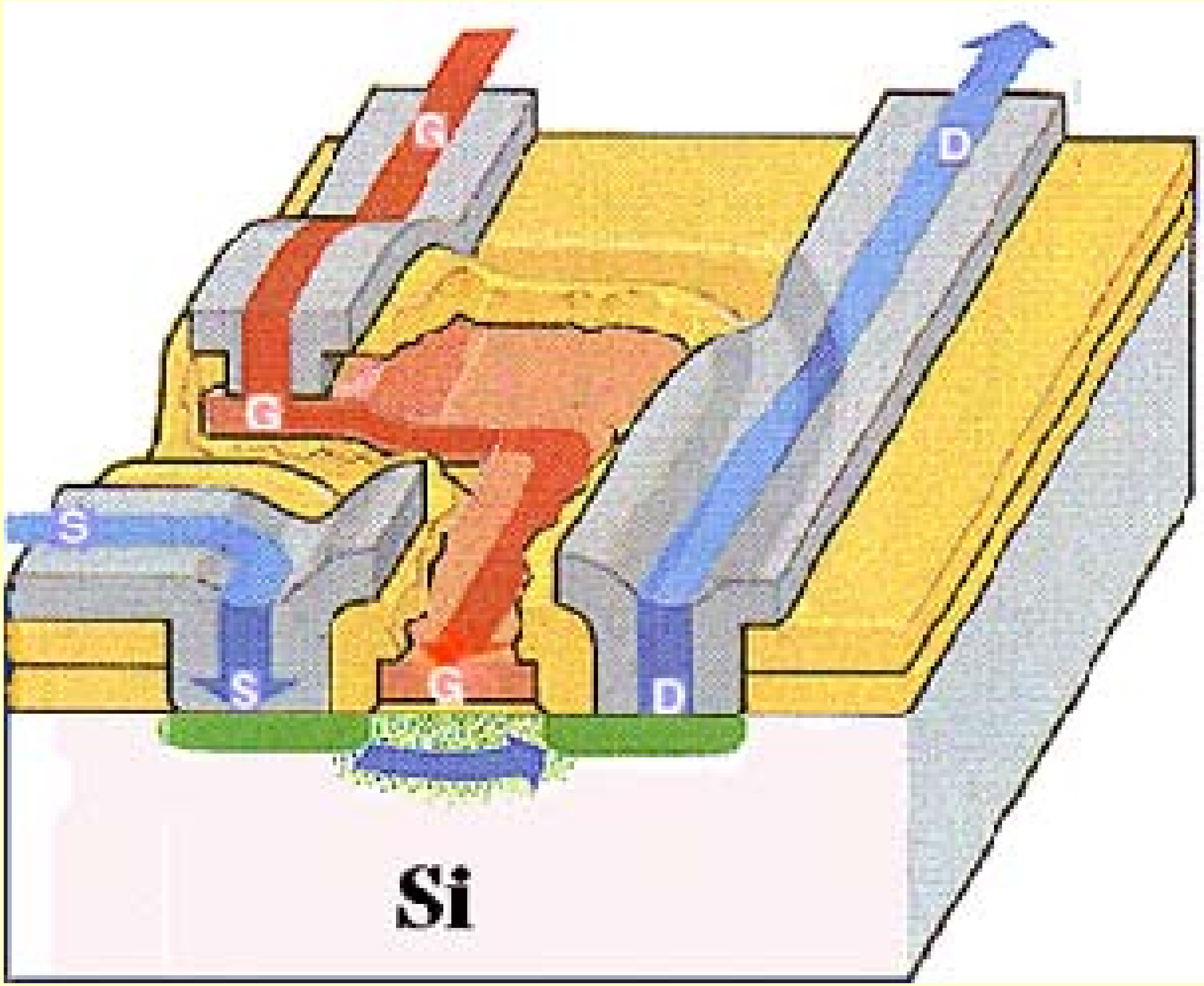




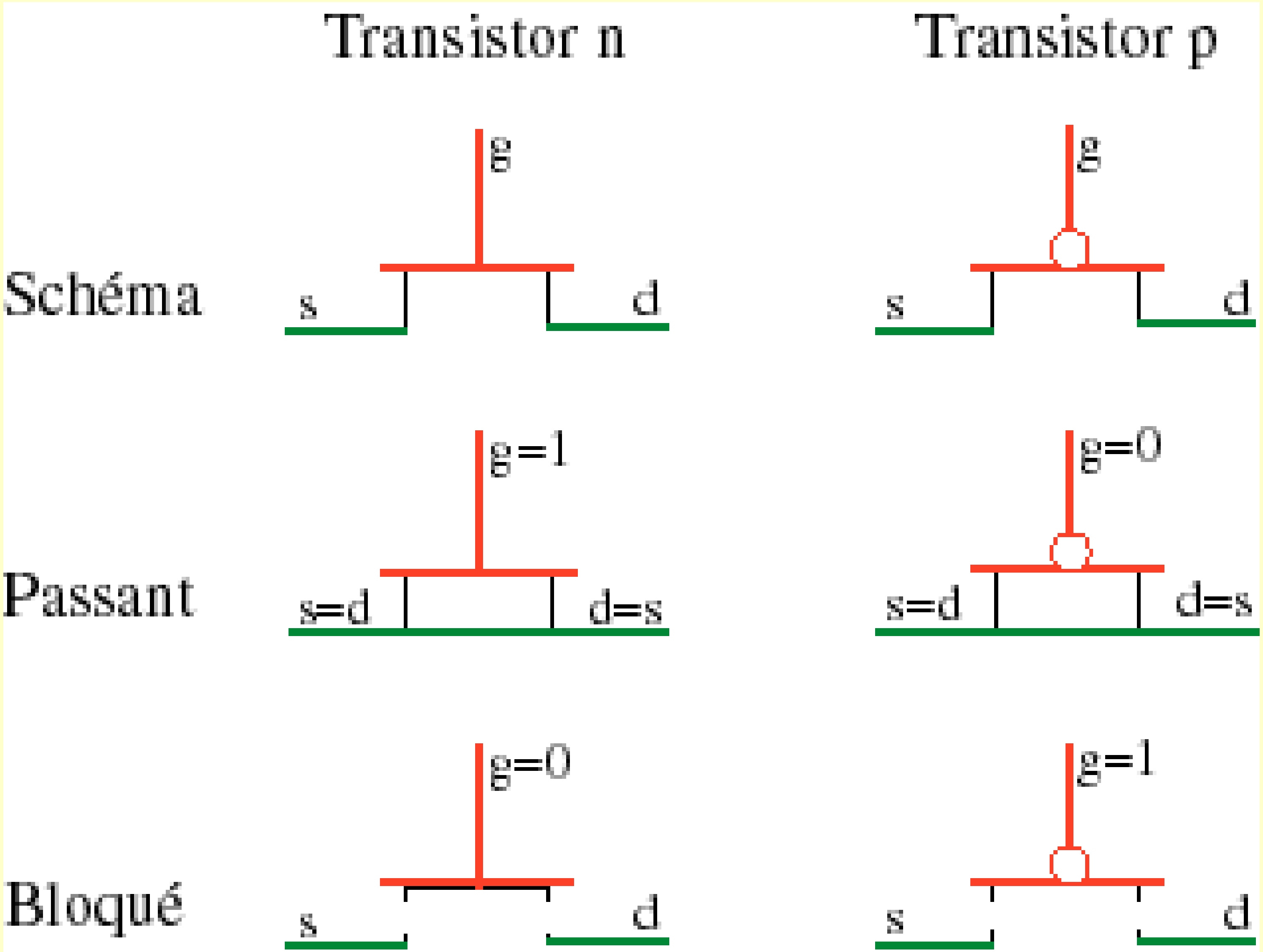
Planar FET





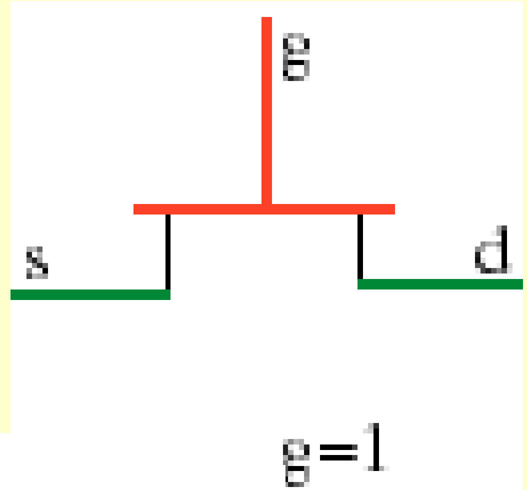


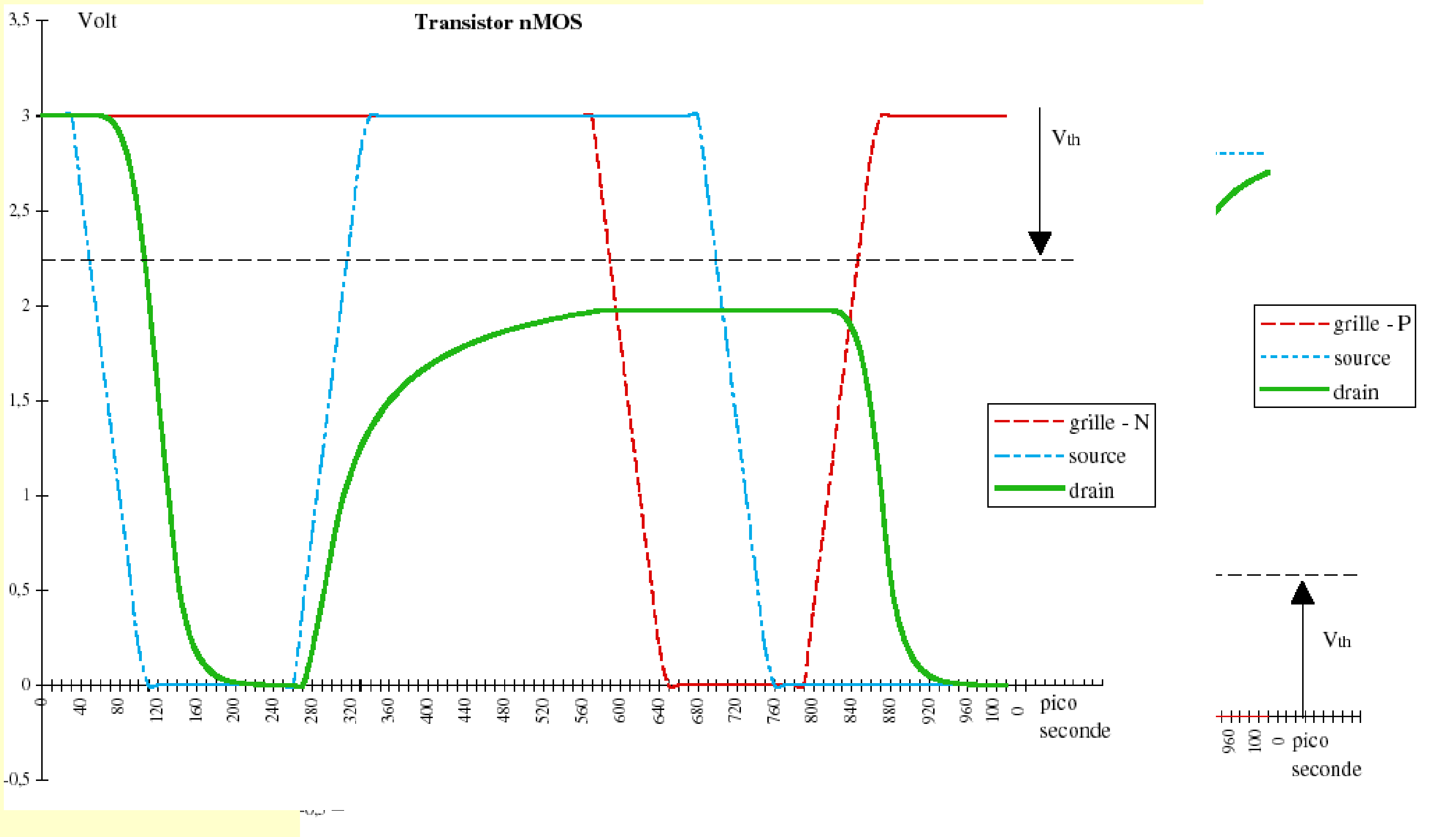
Digital Transistor



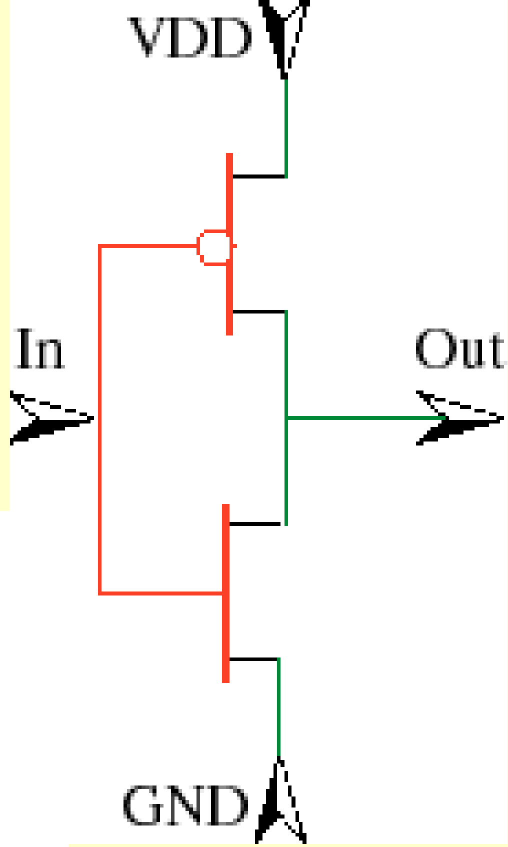
cMOS Transistor

- **Blocked:** $V_{gd} < V_{th}$ $\quad I_{sd}=0$
- **Resistive:** $V_{gd} - V_{th} > V_{sd}$ $\quad I_{sd}=c_n\,(V_{gd} - V_{th})^2$
- **Saturated:** $V_{gd} - V_{th} < V_{sd}$ $\quad I_{sd}=c_n\,(V_{gd} - V_{th})^2/2$

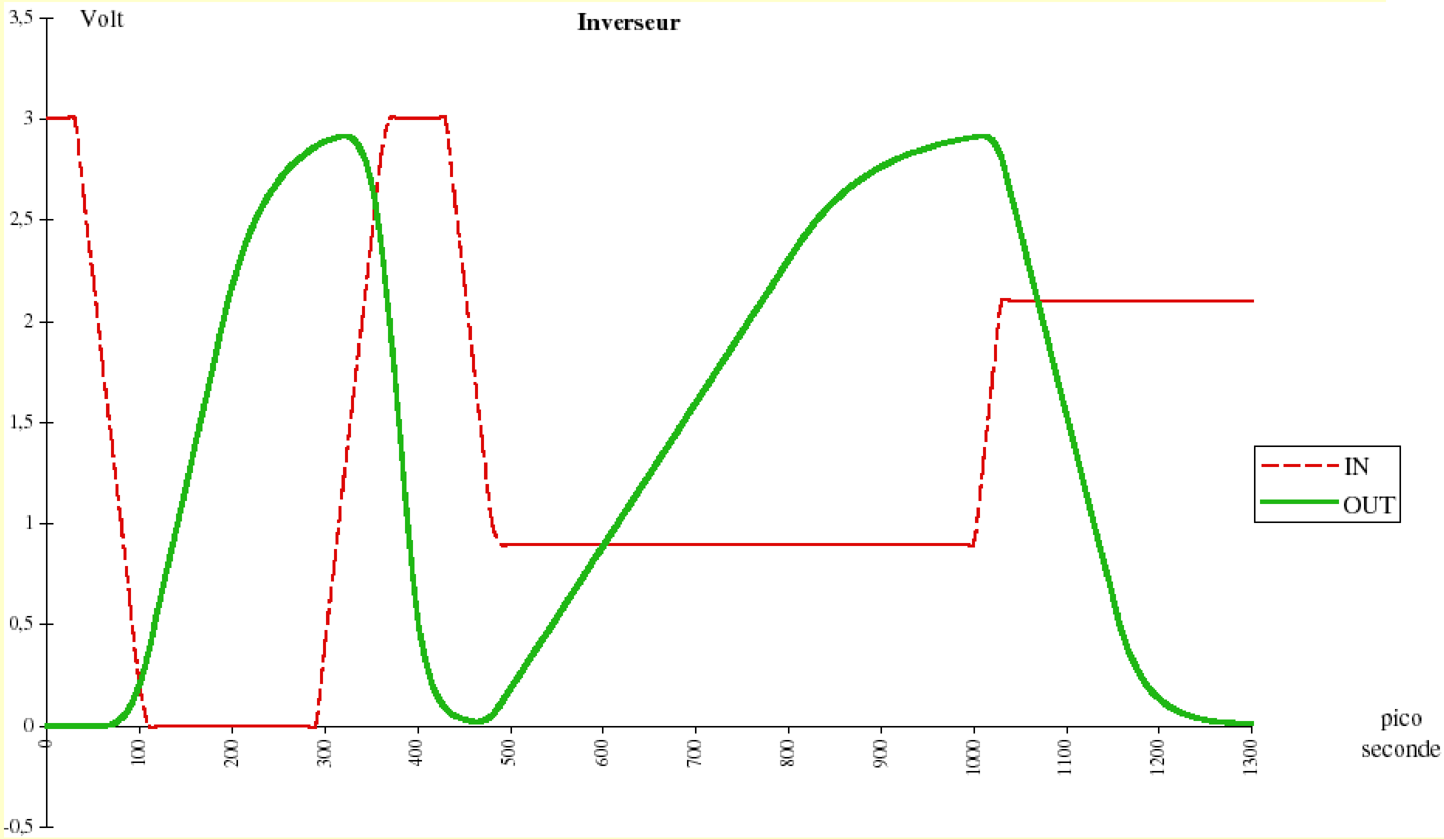




Invert

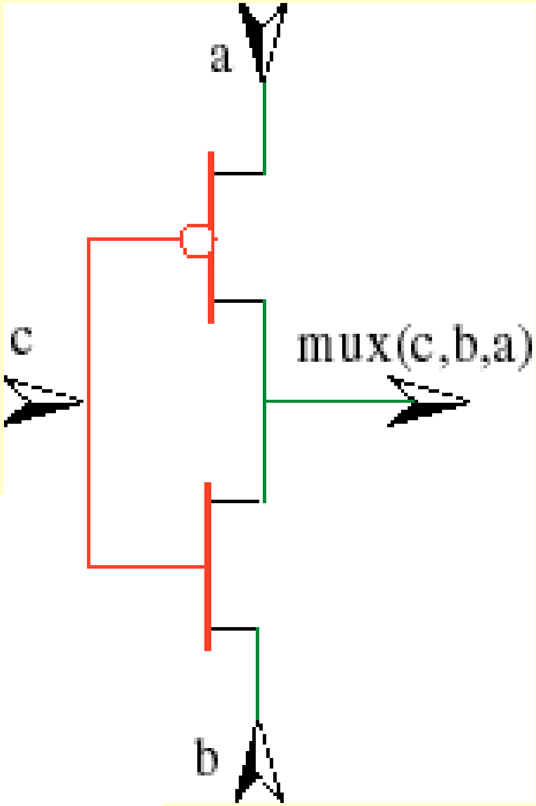


VDD
In
Out
GND

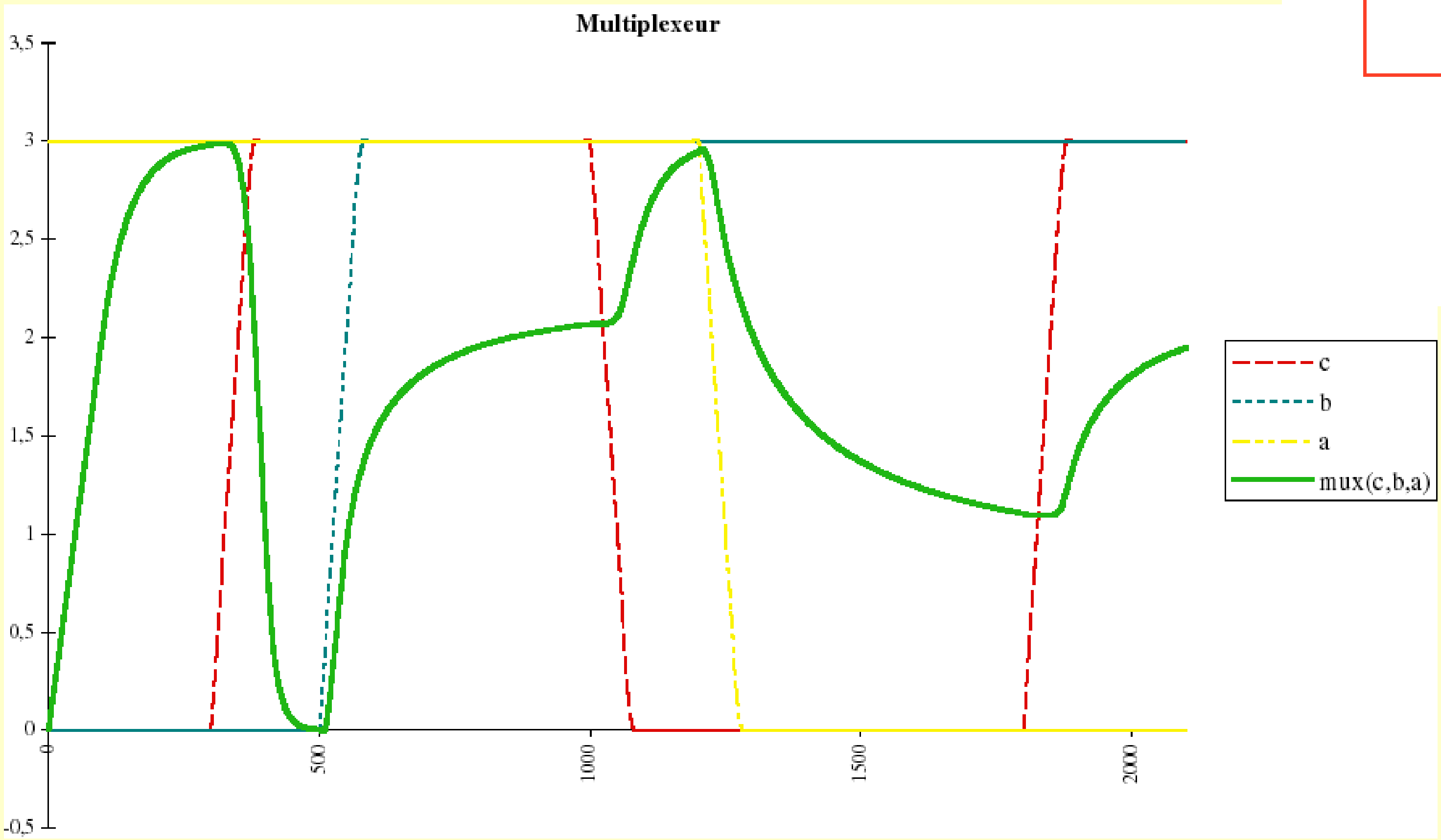


Inverseur
Volt
3,5
3
2,5
2
1,5
1
0,5
0
-0,5
0
100
200
300
400
500
600
700
800
900
1000
1100
1200
1300
pico seconde
IN
OUT

Multiplex

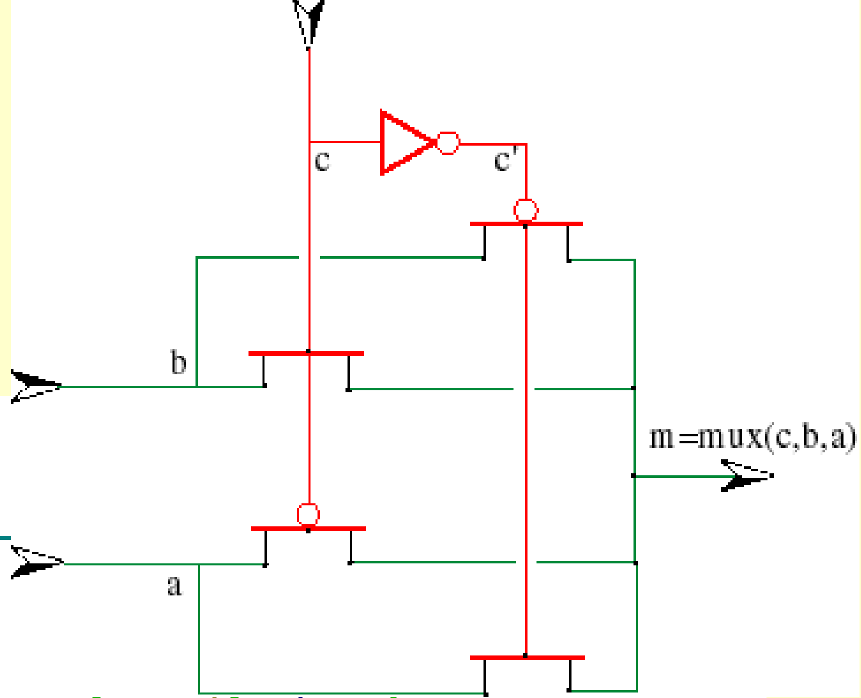


a
c
mux(c,b,a)
b

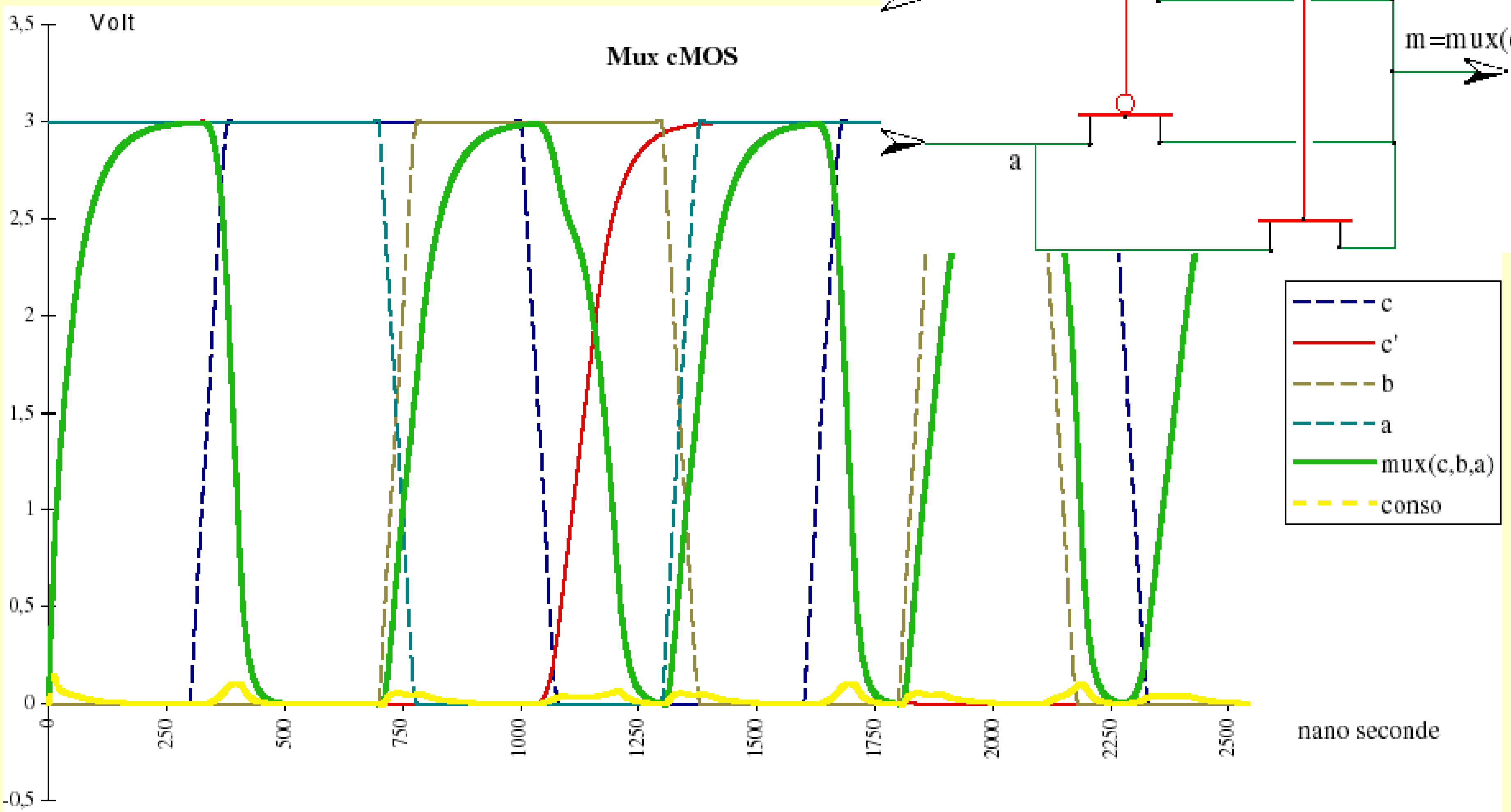


Multiplexeur
3,5
3
2,5
2
1,5
1
0,5
0
-0,5
0
500
1000
1500
2000
c
b
a
mux(c,b,a)

cMOS MUX

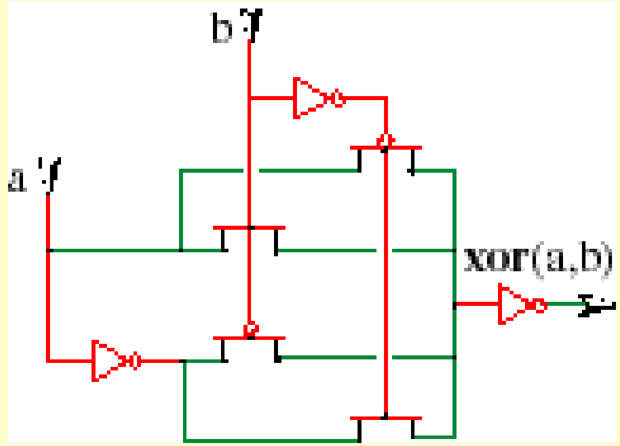


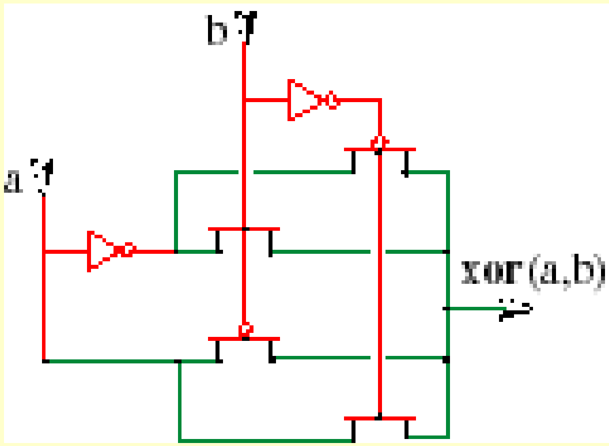
c
c'
b
a
m=mux(c,b,a)



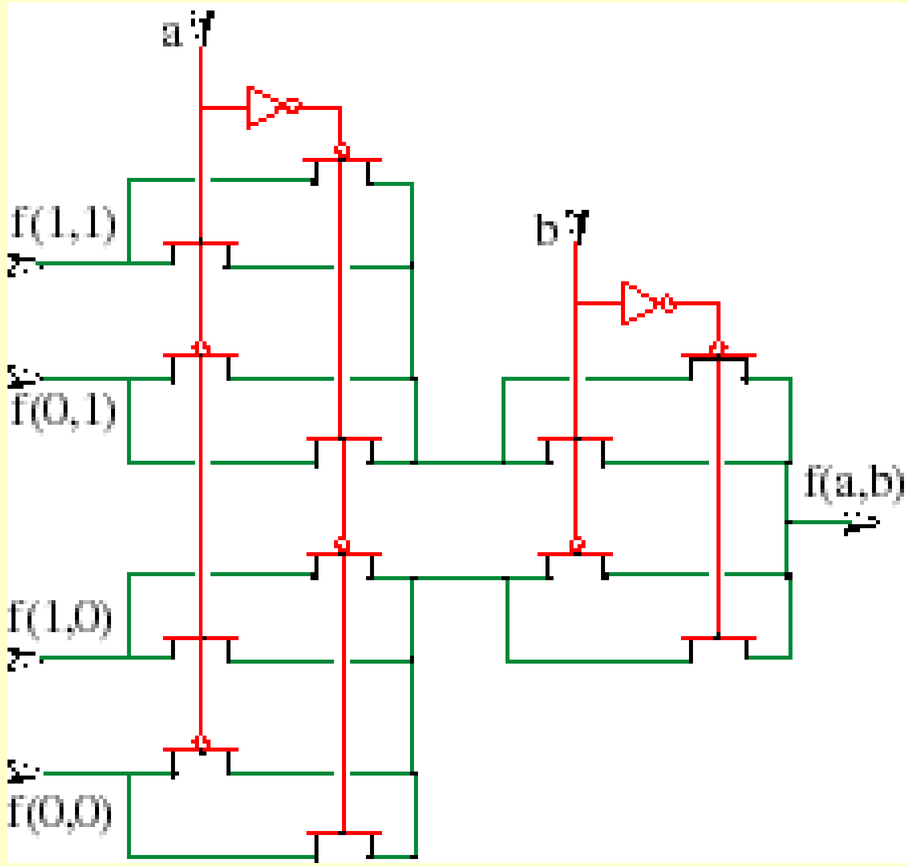
Volt
Mux cMOS
3,5
3
2,5
2
1,5
1
0,5
0
-0,5
0
250
500
750
1000
1250
1500
1750
2000
2250
2500
nano seconde
c
c'
b
a
mux(c,b,a)
conso

cMOS XOR

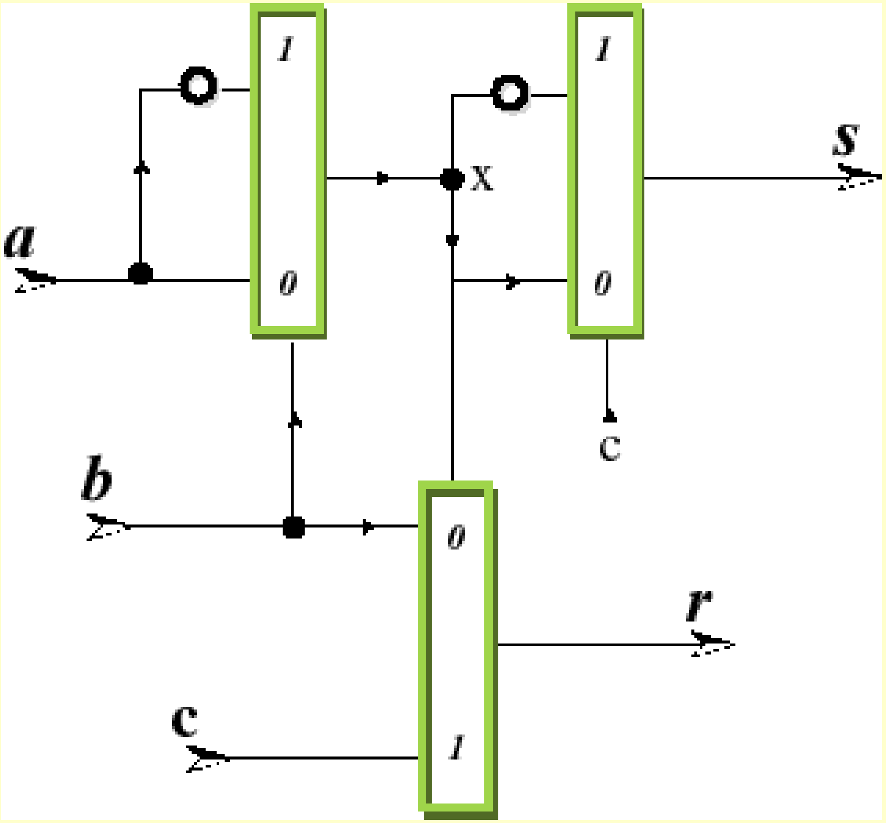


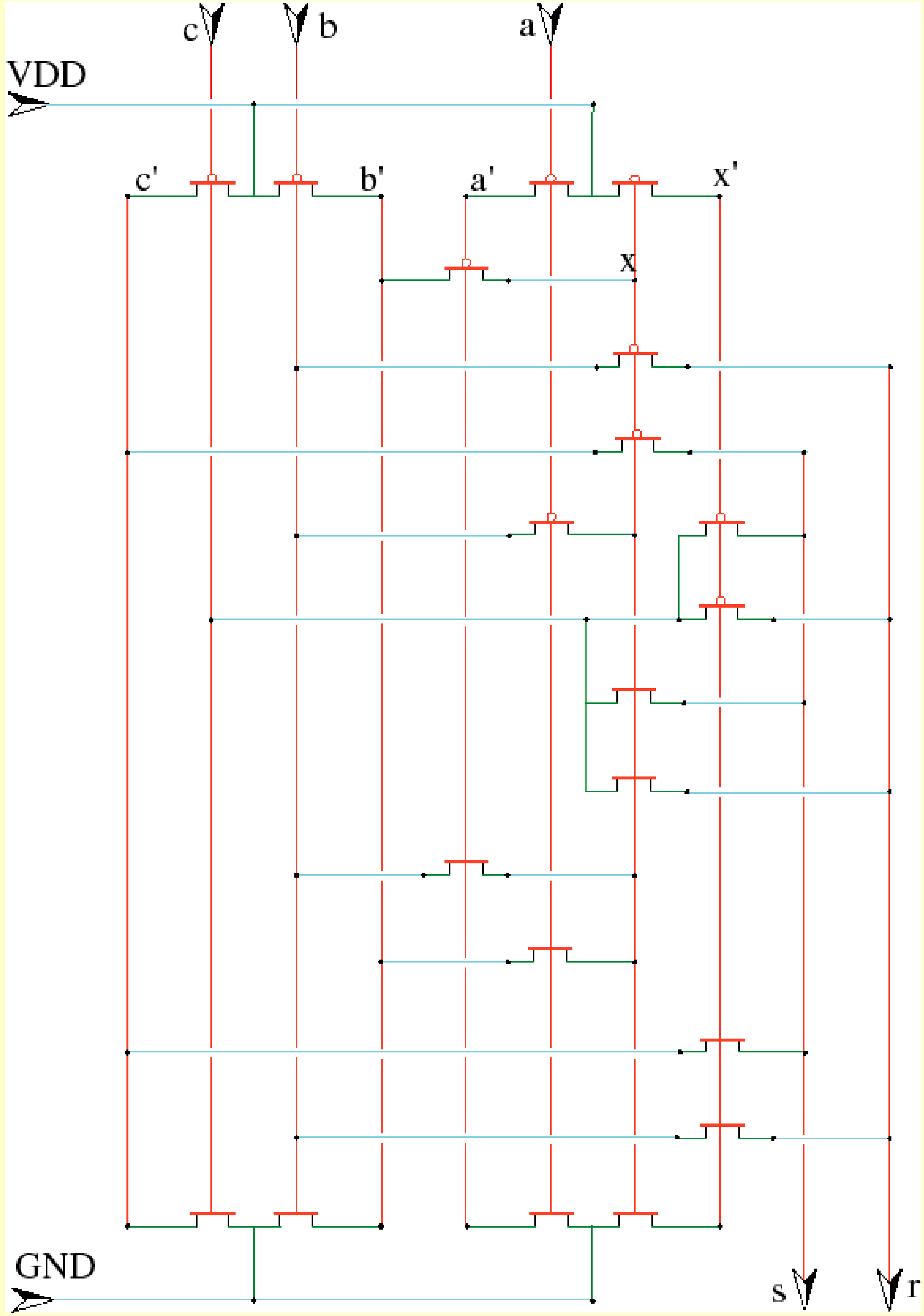


cMOS LUT2



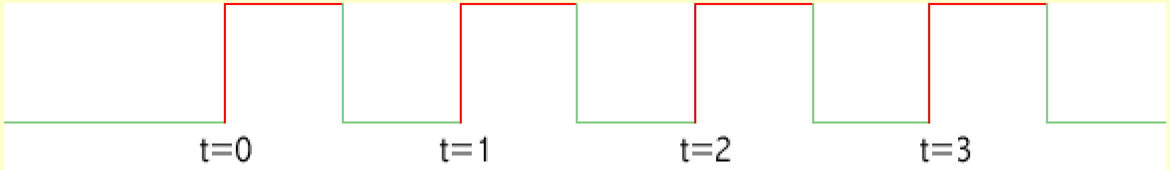
Custom Full Adder

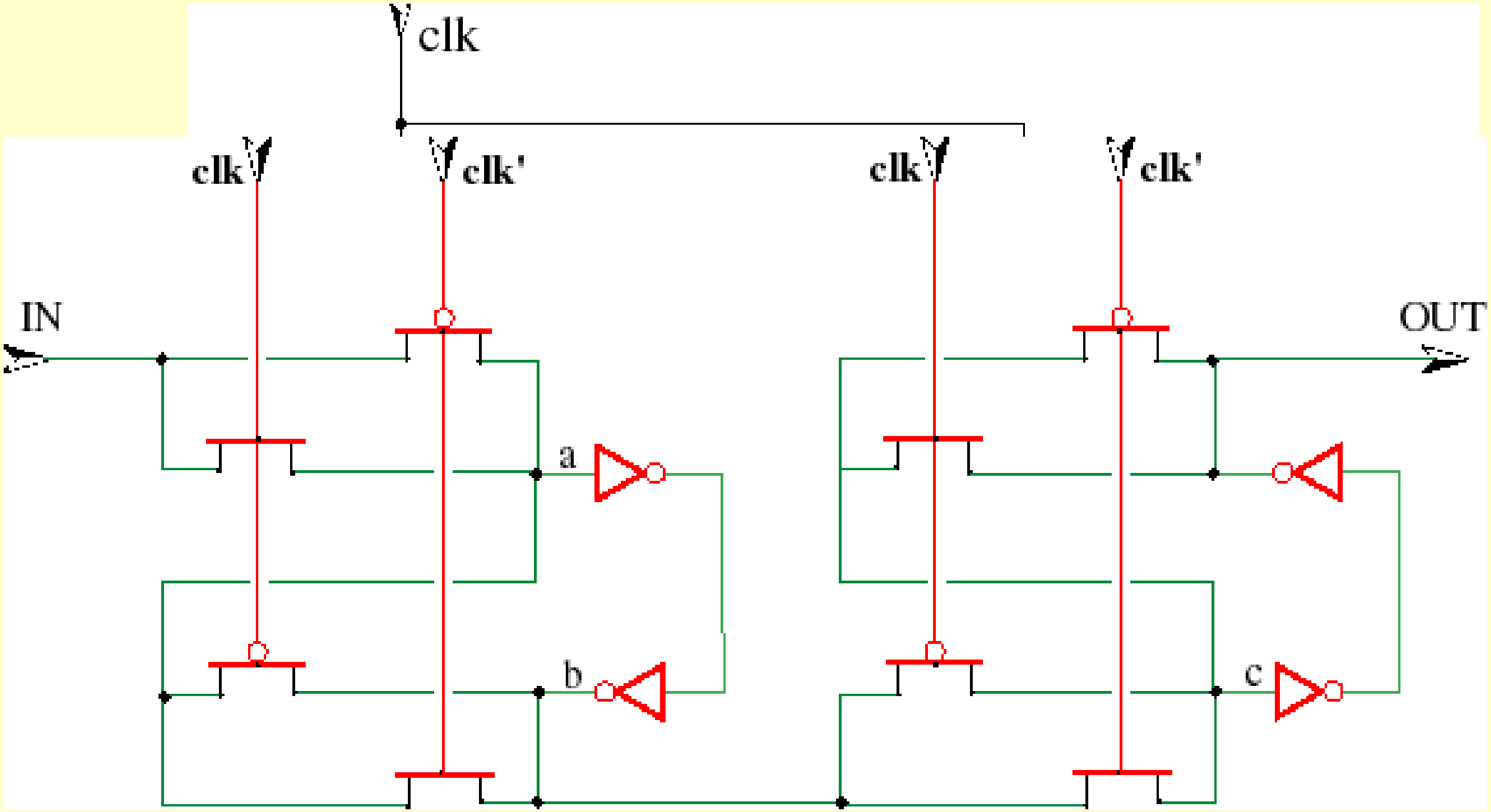




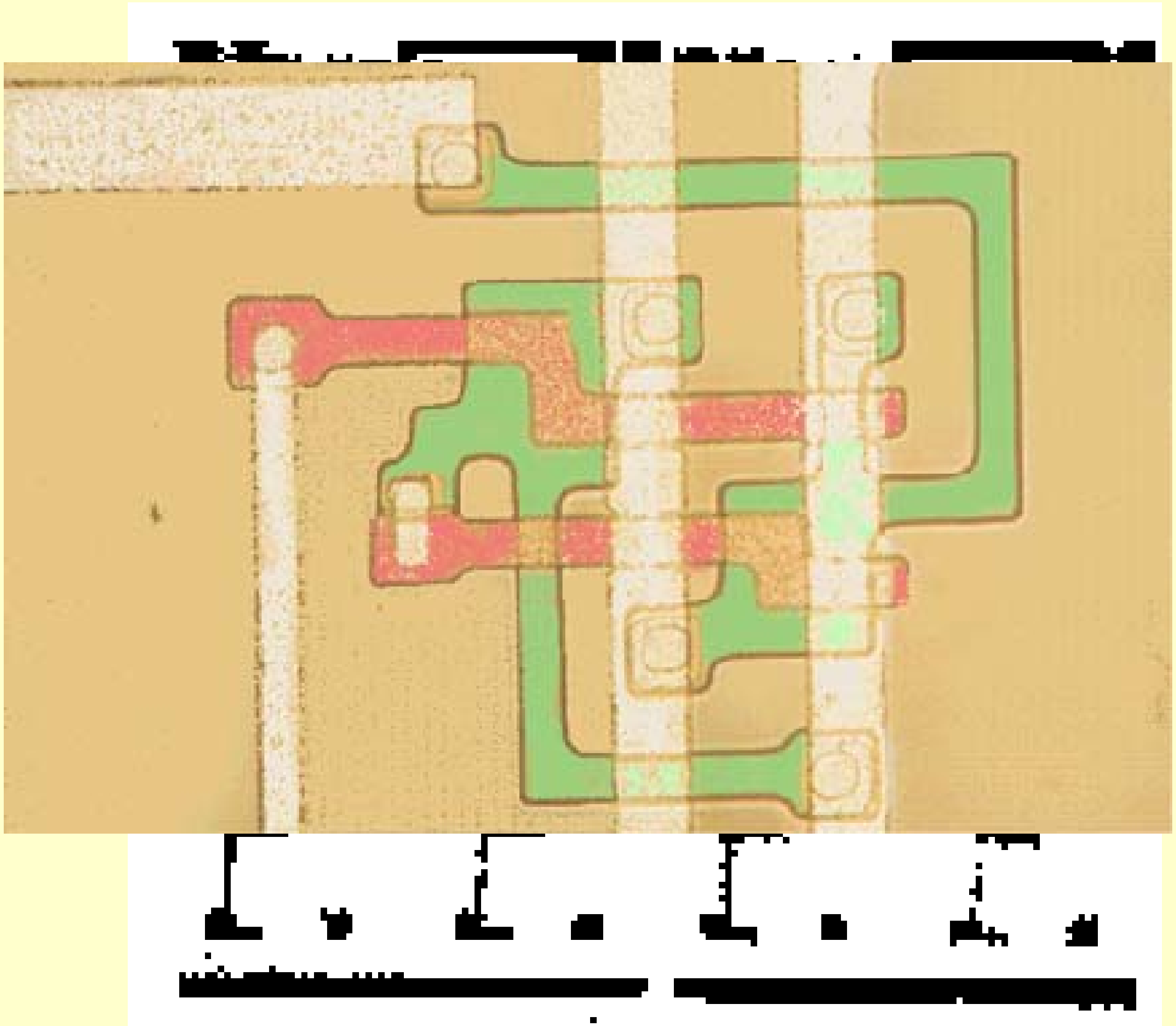
Digital Time & Register

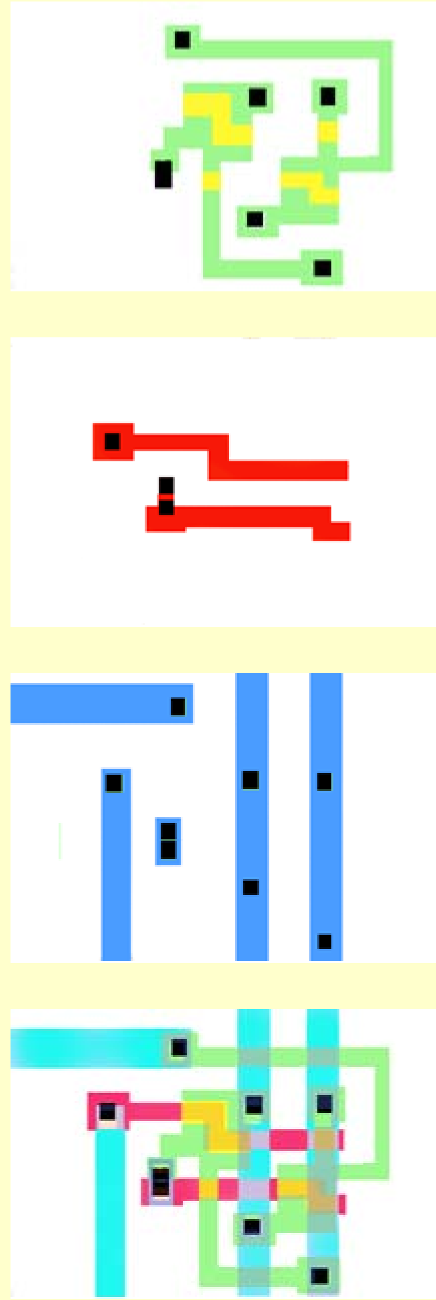
$$clk(t) = \sum_{n\in\mathbb{N}} \partial(t-n)$$



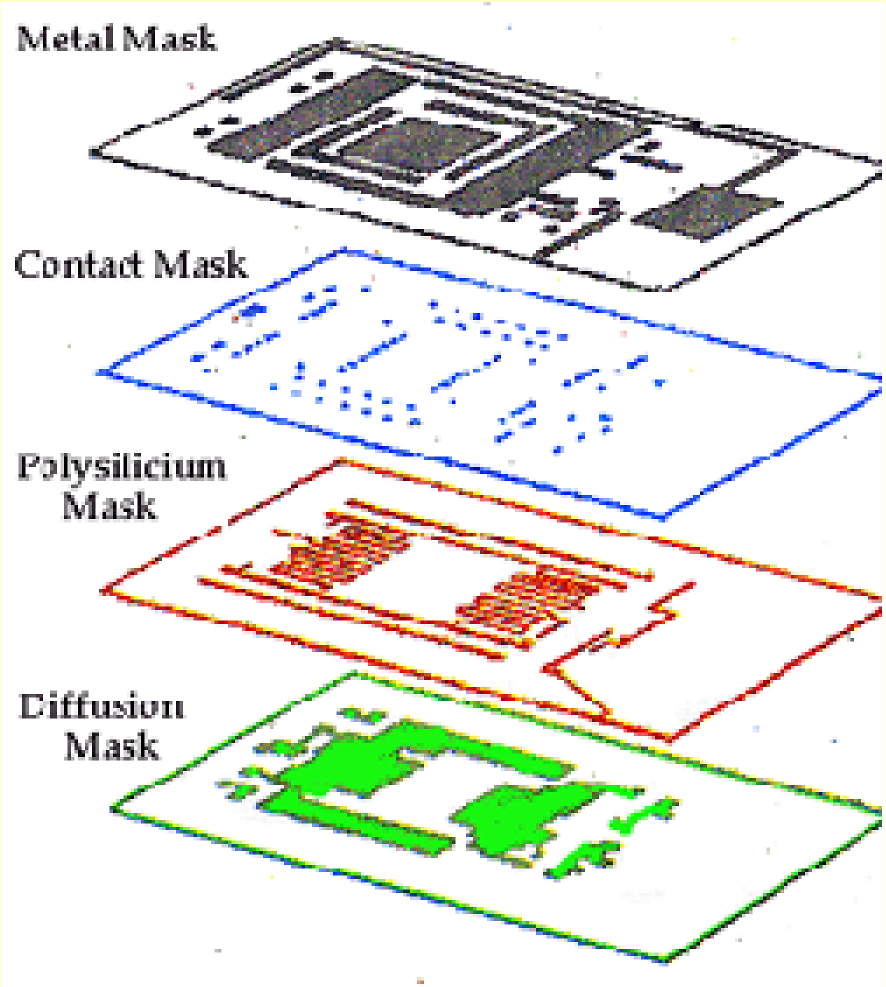


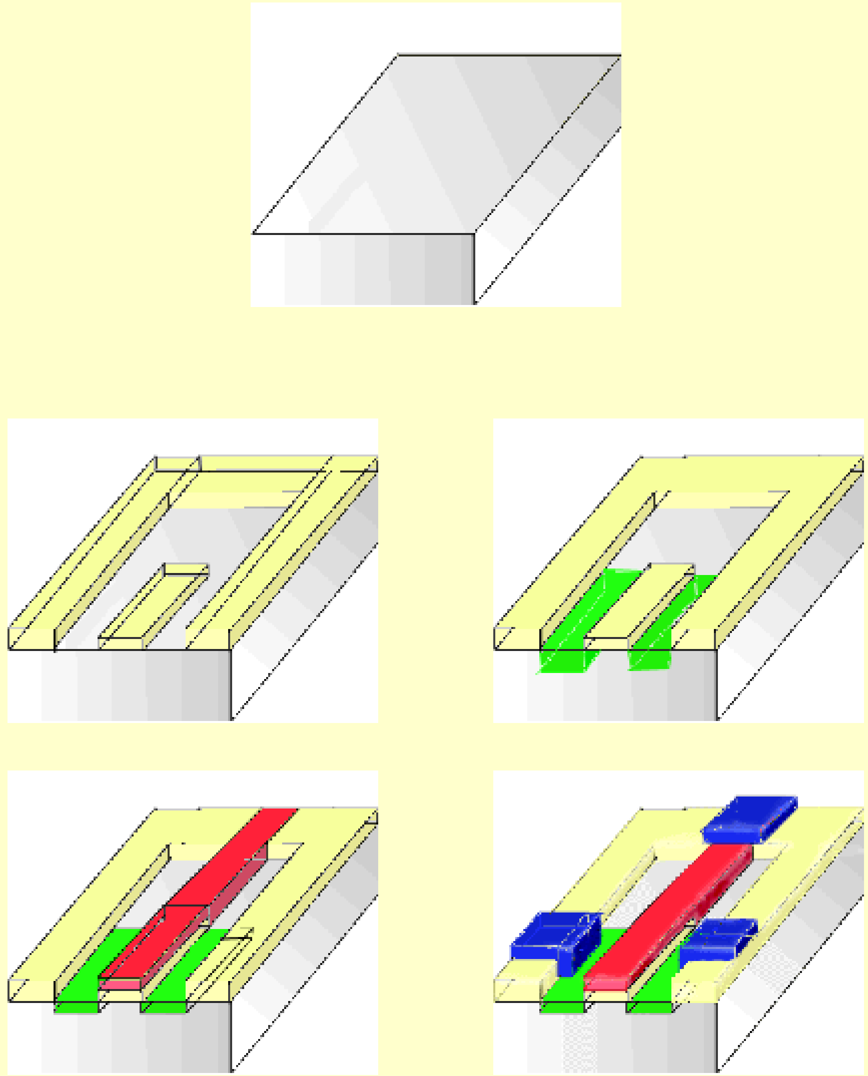
Masks



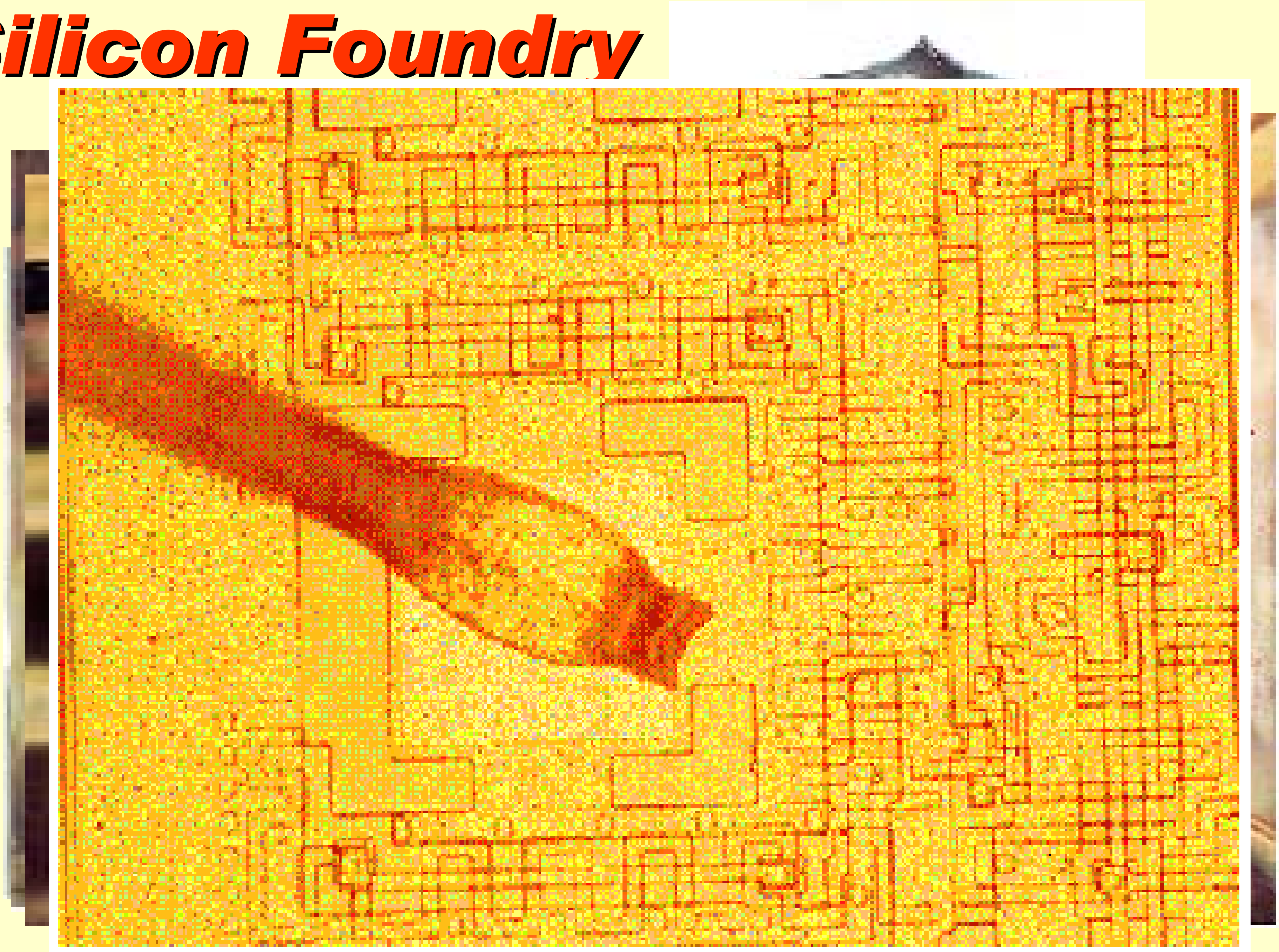


MOS Process

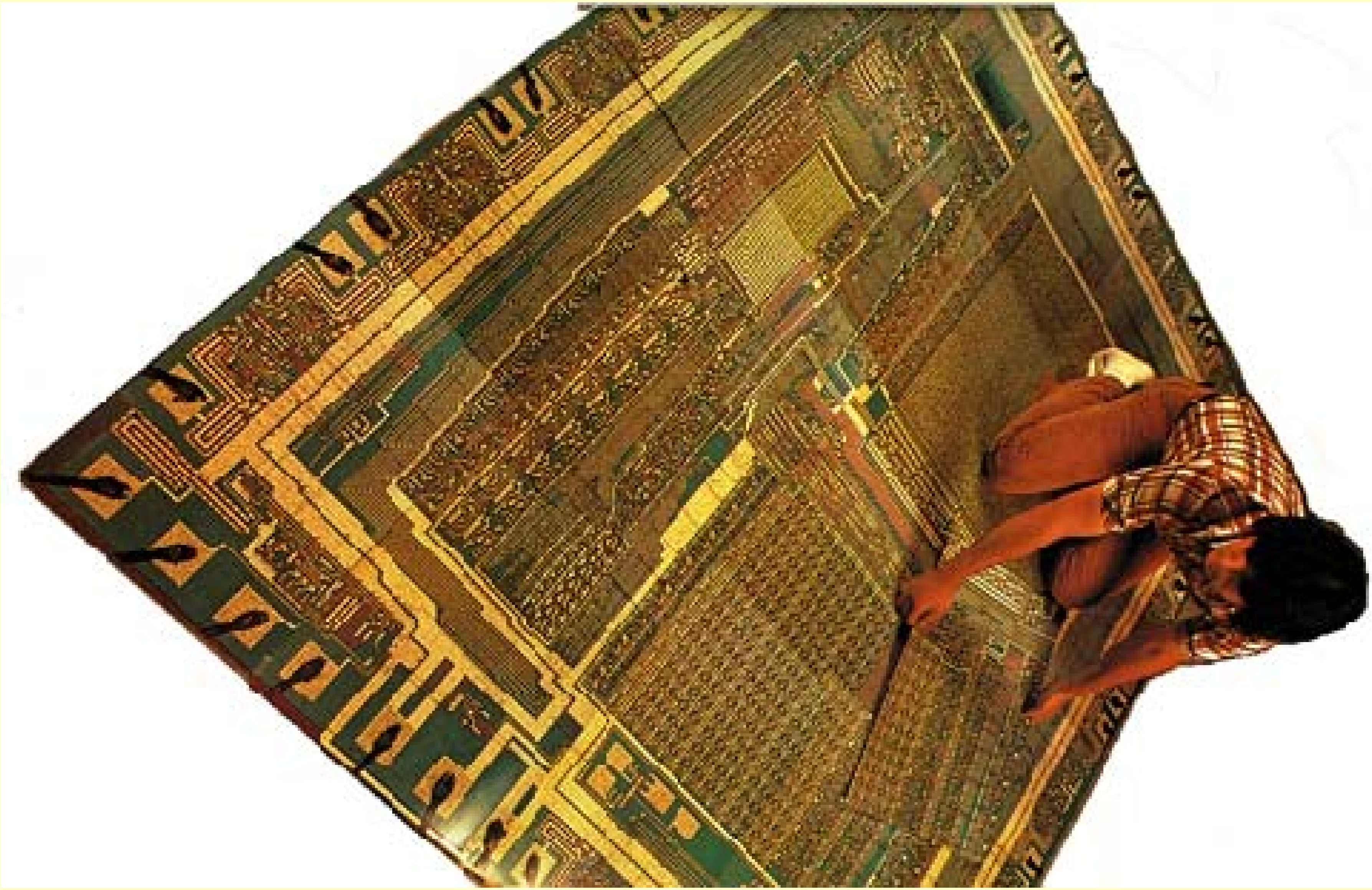




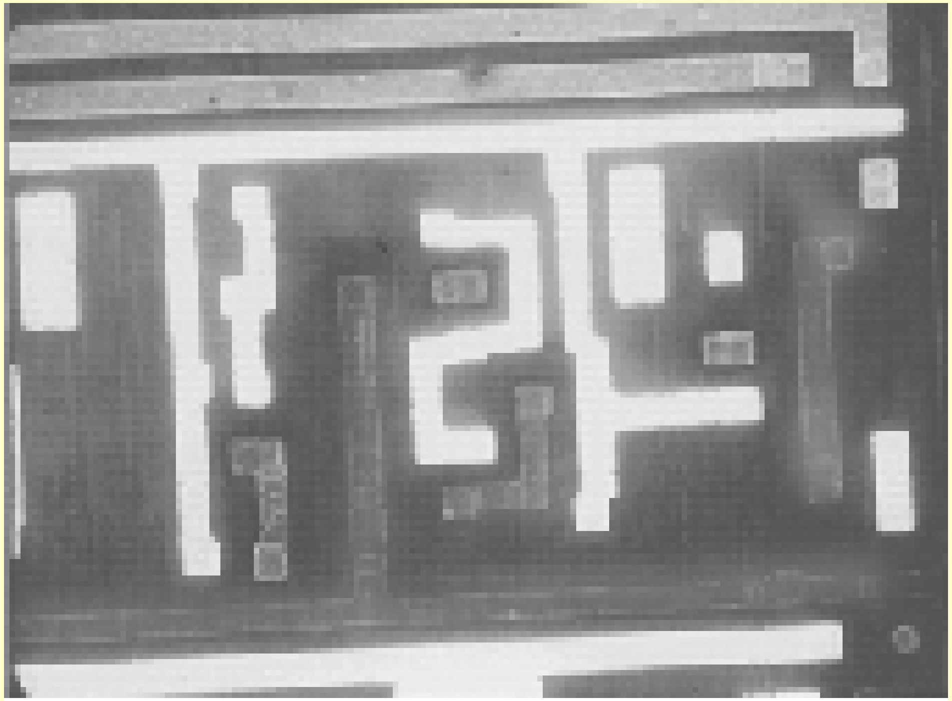
Silicon Foundry

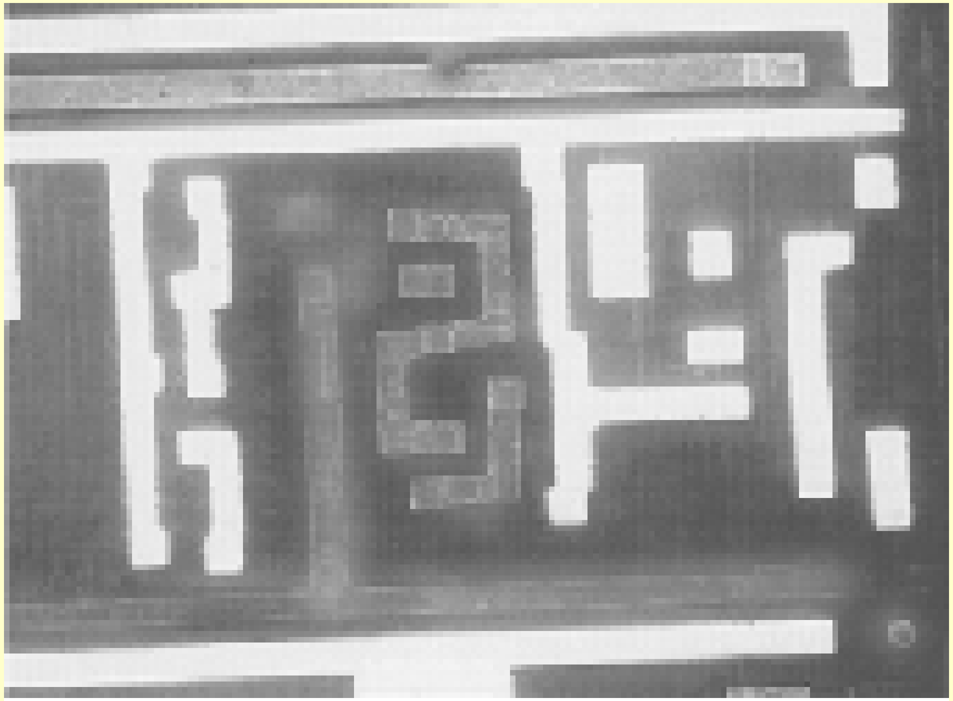


Floor Plan

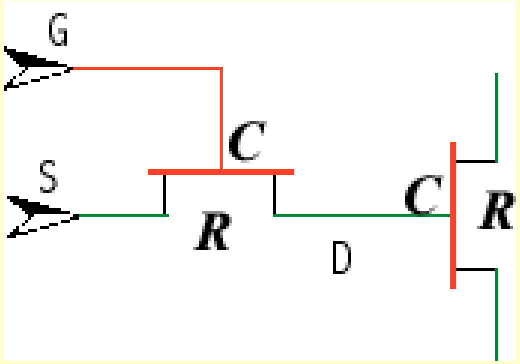


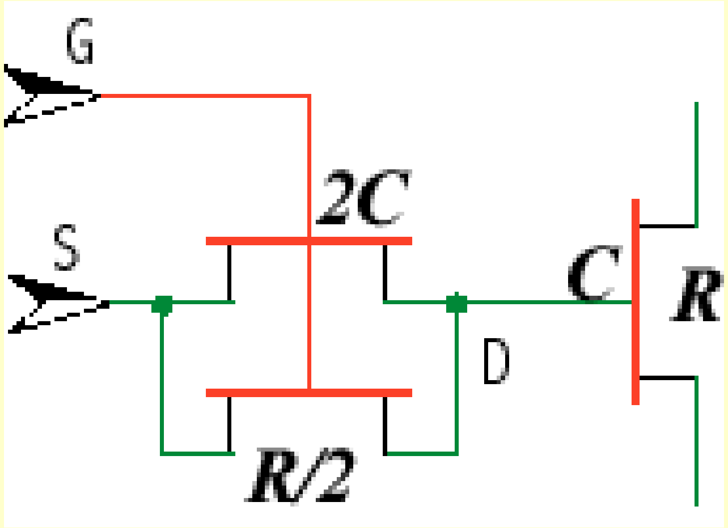
EBM

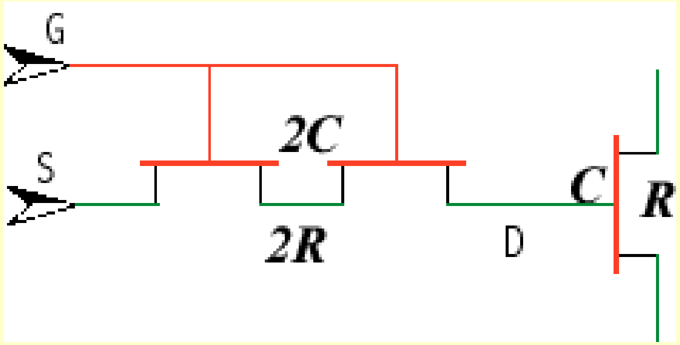


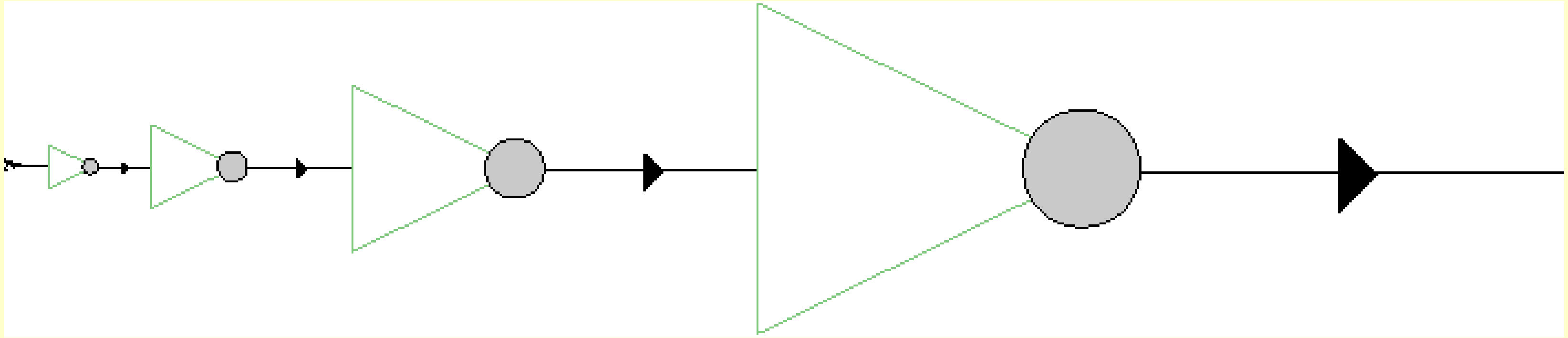


Delays: RC Model

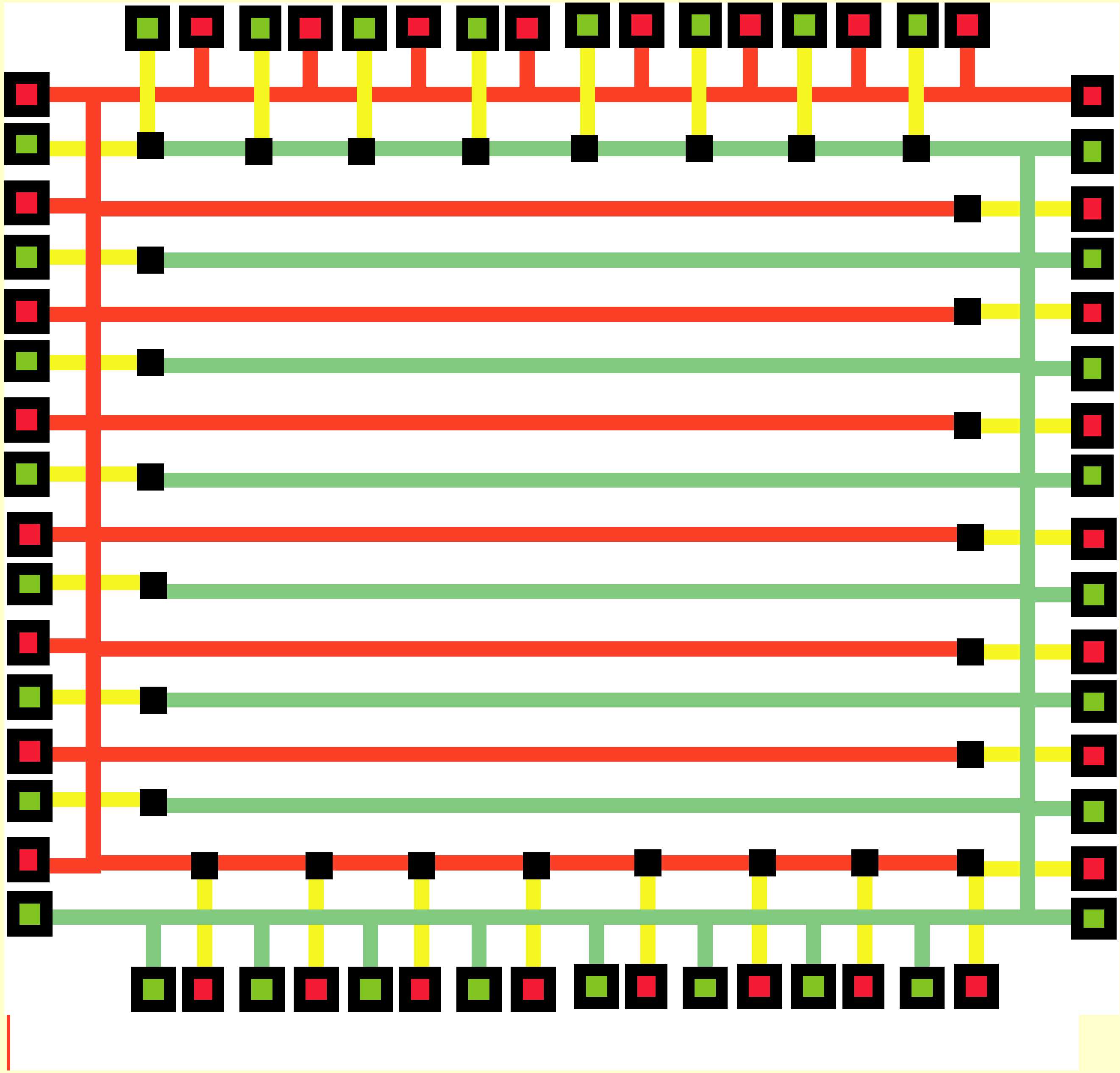




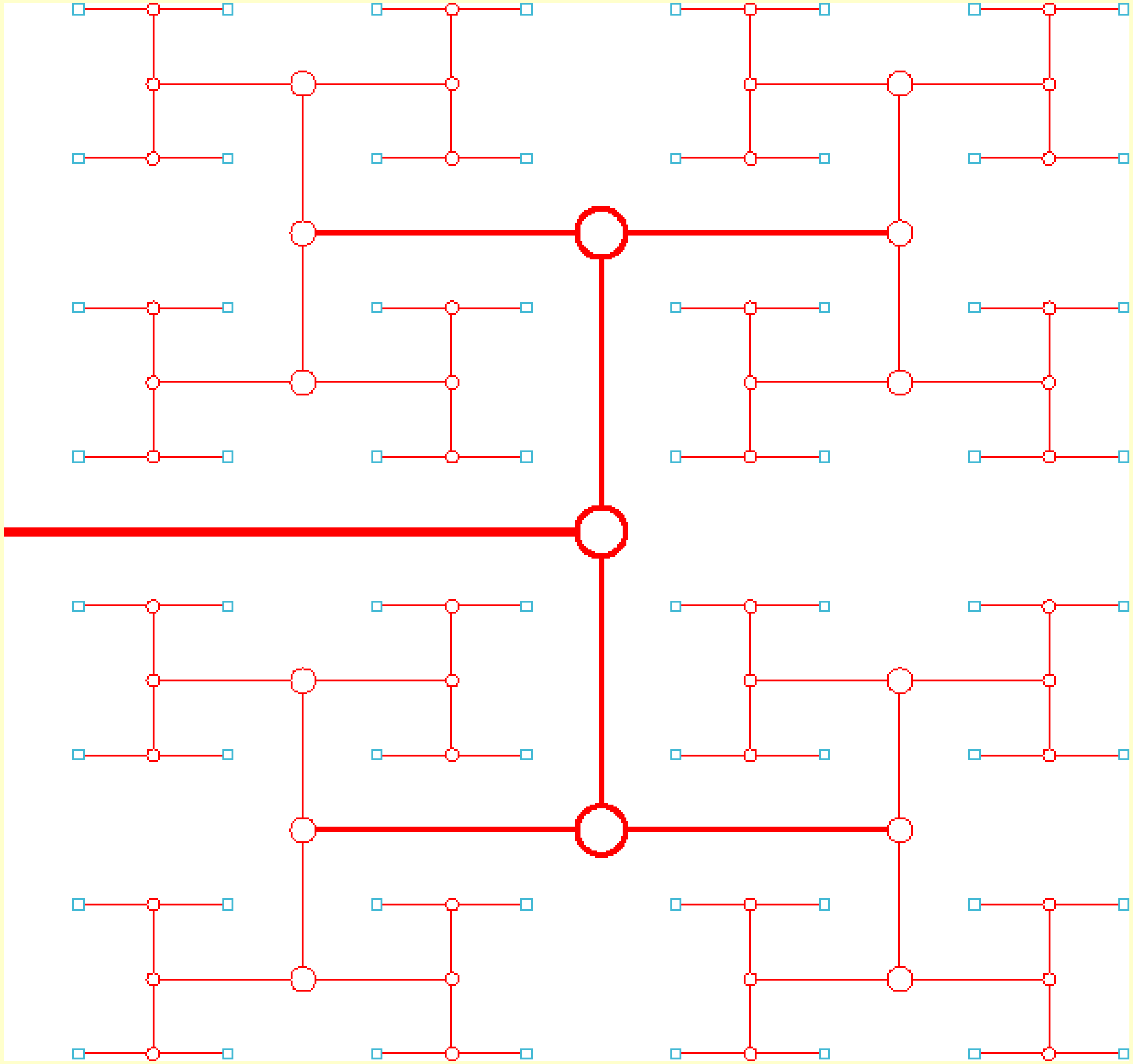




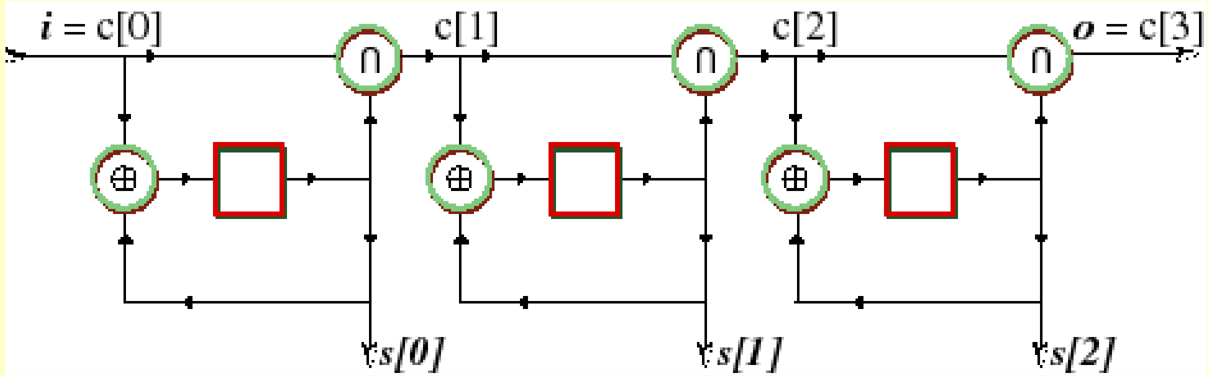
Power

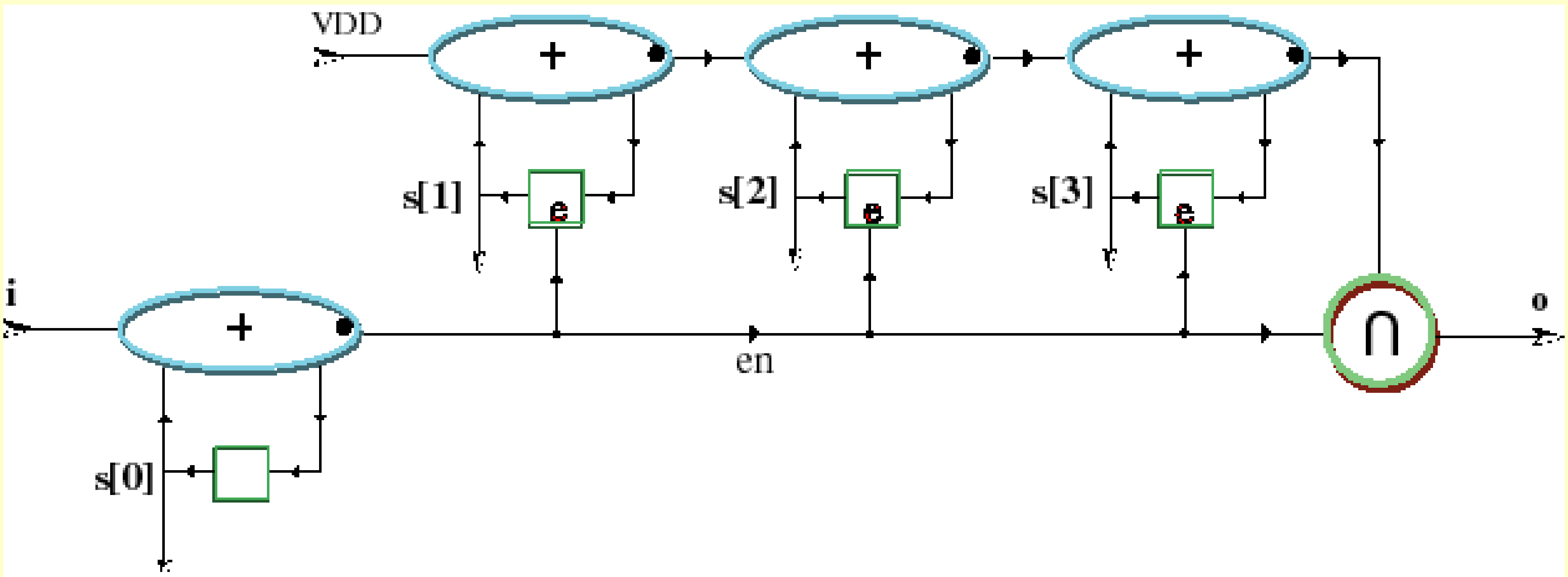


Clock

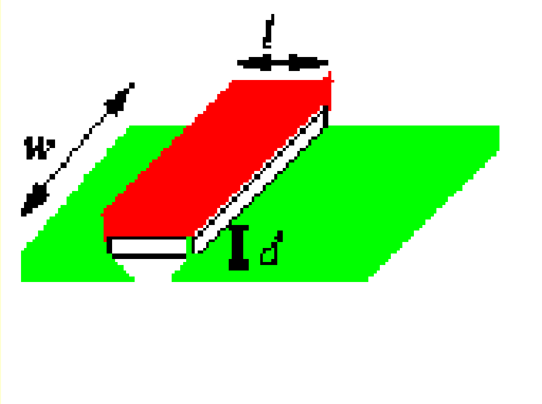


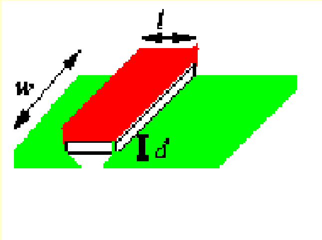
Fast Counter





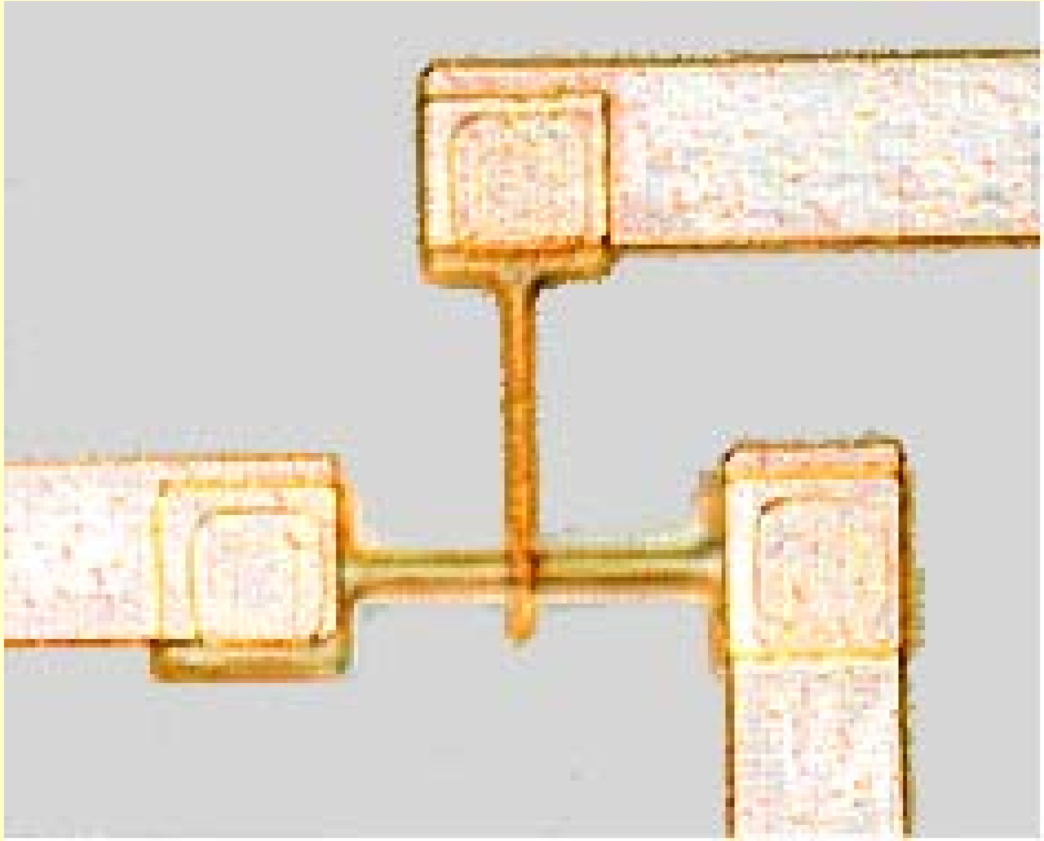
Shrink Laws



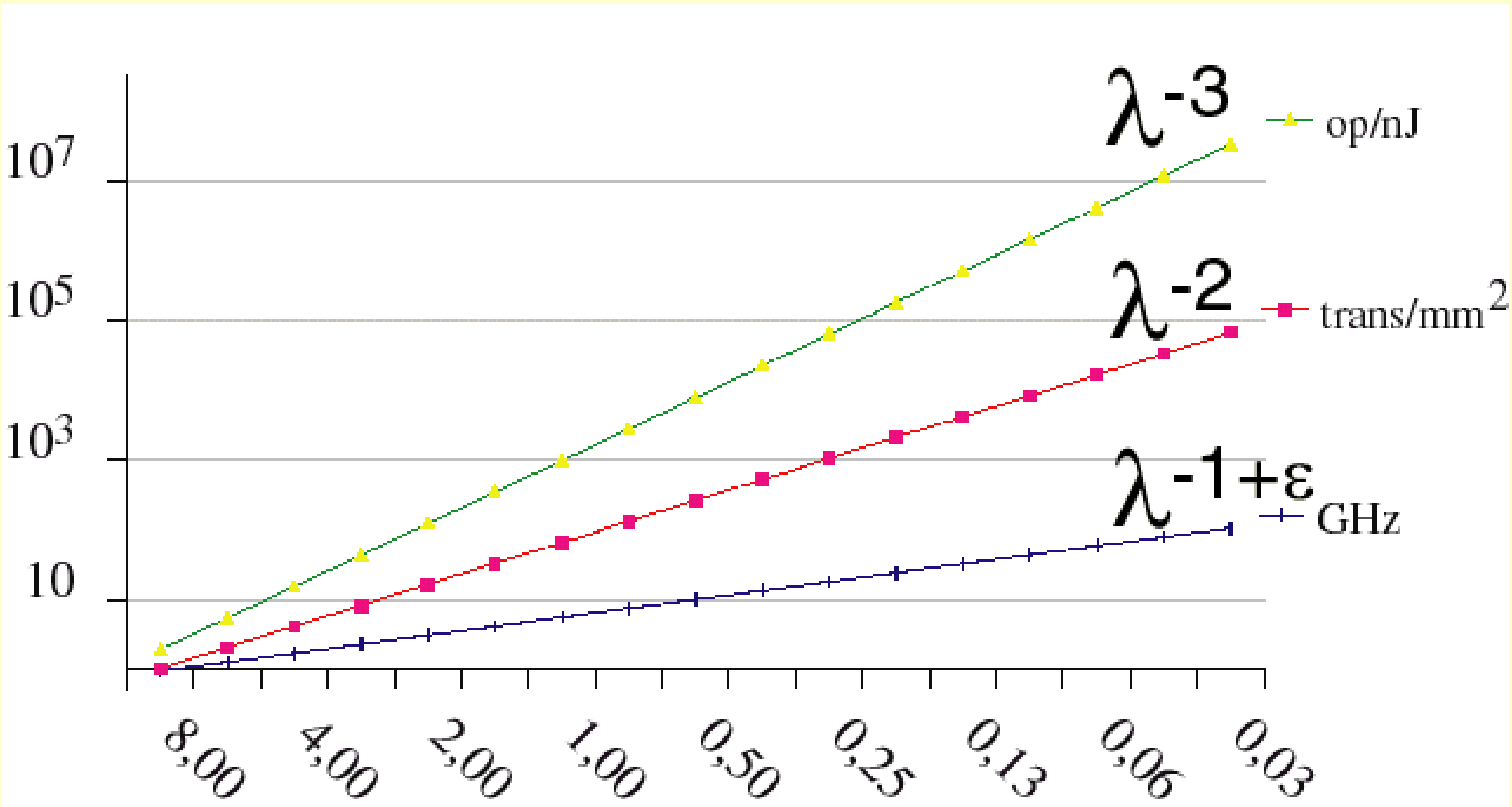


Gains

- Size
- Speed
- Power
- Reliability
- Cost

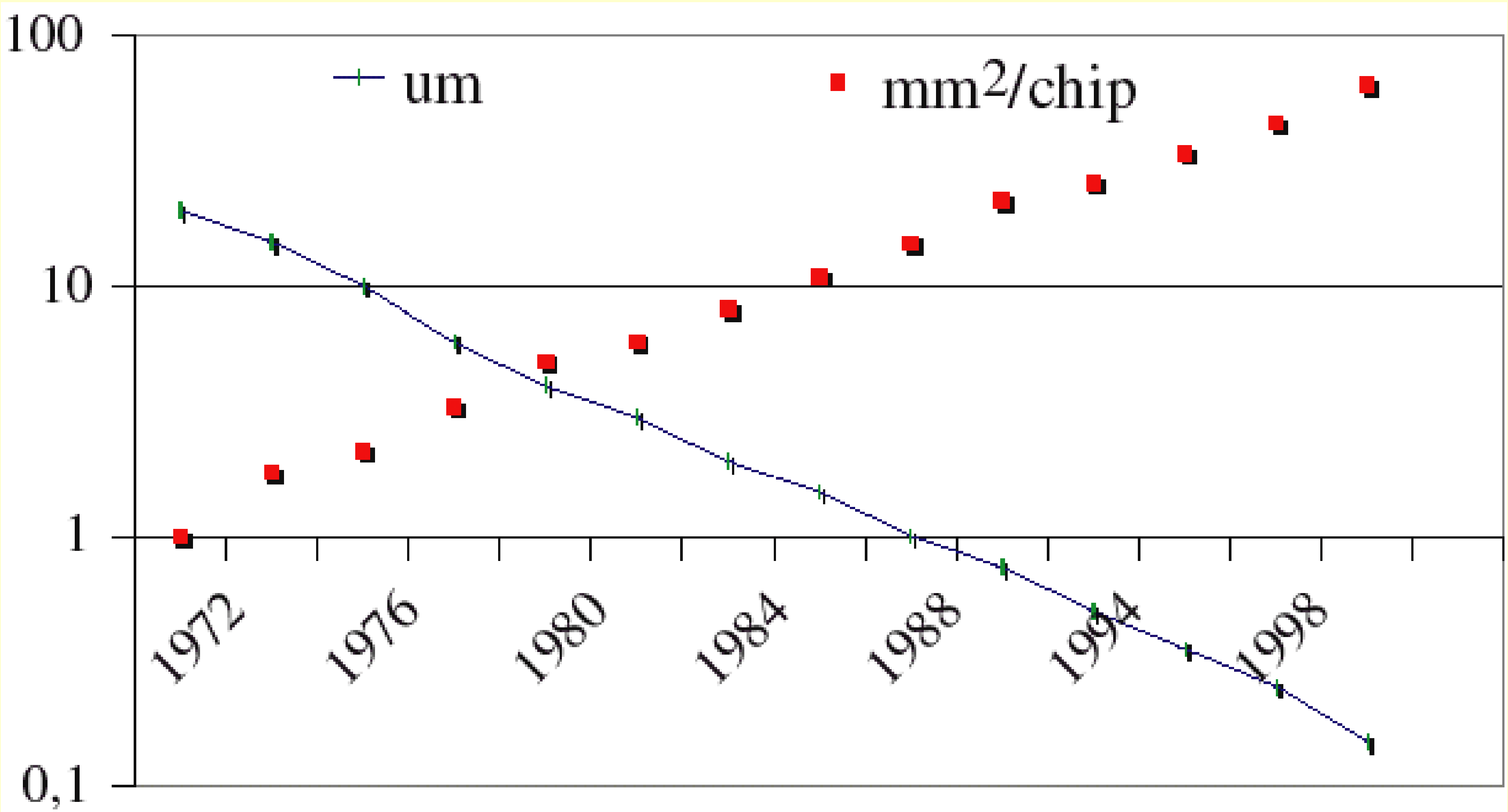


Shrink

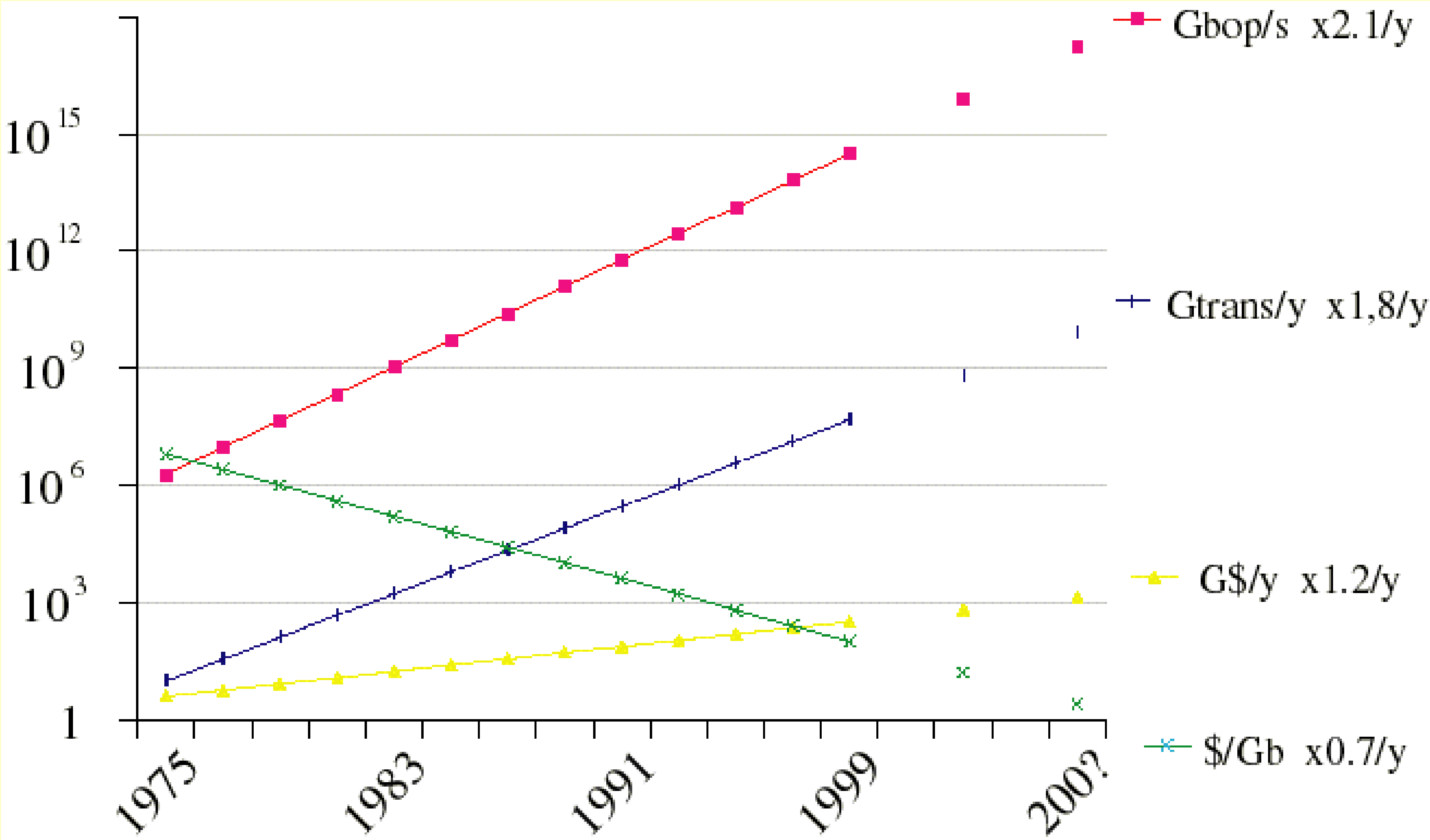


10^7
10^5
10^3
10
λ^{-3}
op/nJ
λ^{-2}
trans/mm^2
$\lambda^{-1+\varepsilon}$
GHz
8,00
4,00
2,00
1,00
0,50
0,25
0,13
0,06
0,03

Chip History

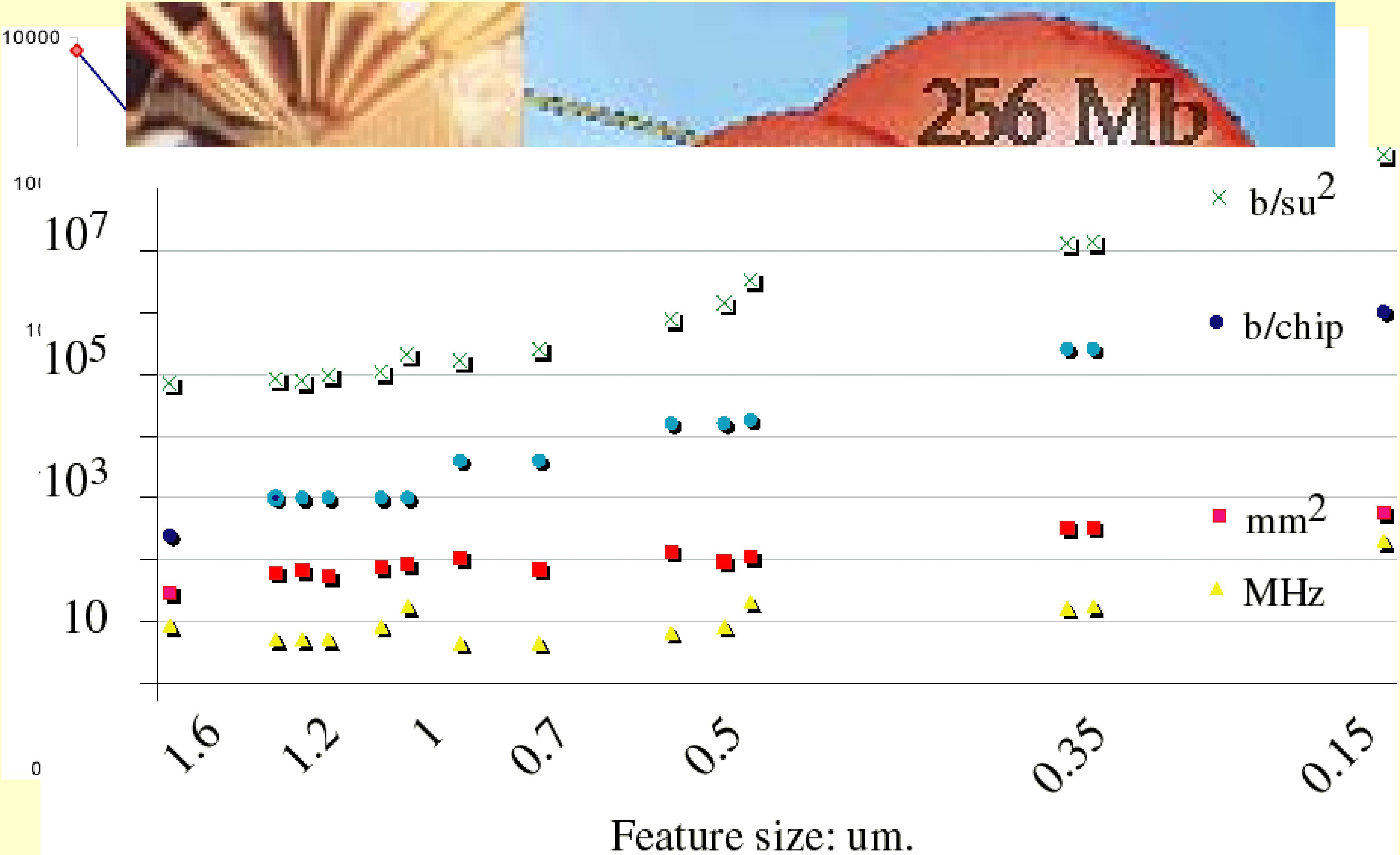


Moore's Laws



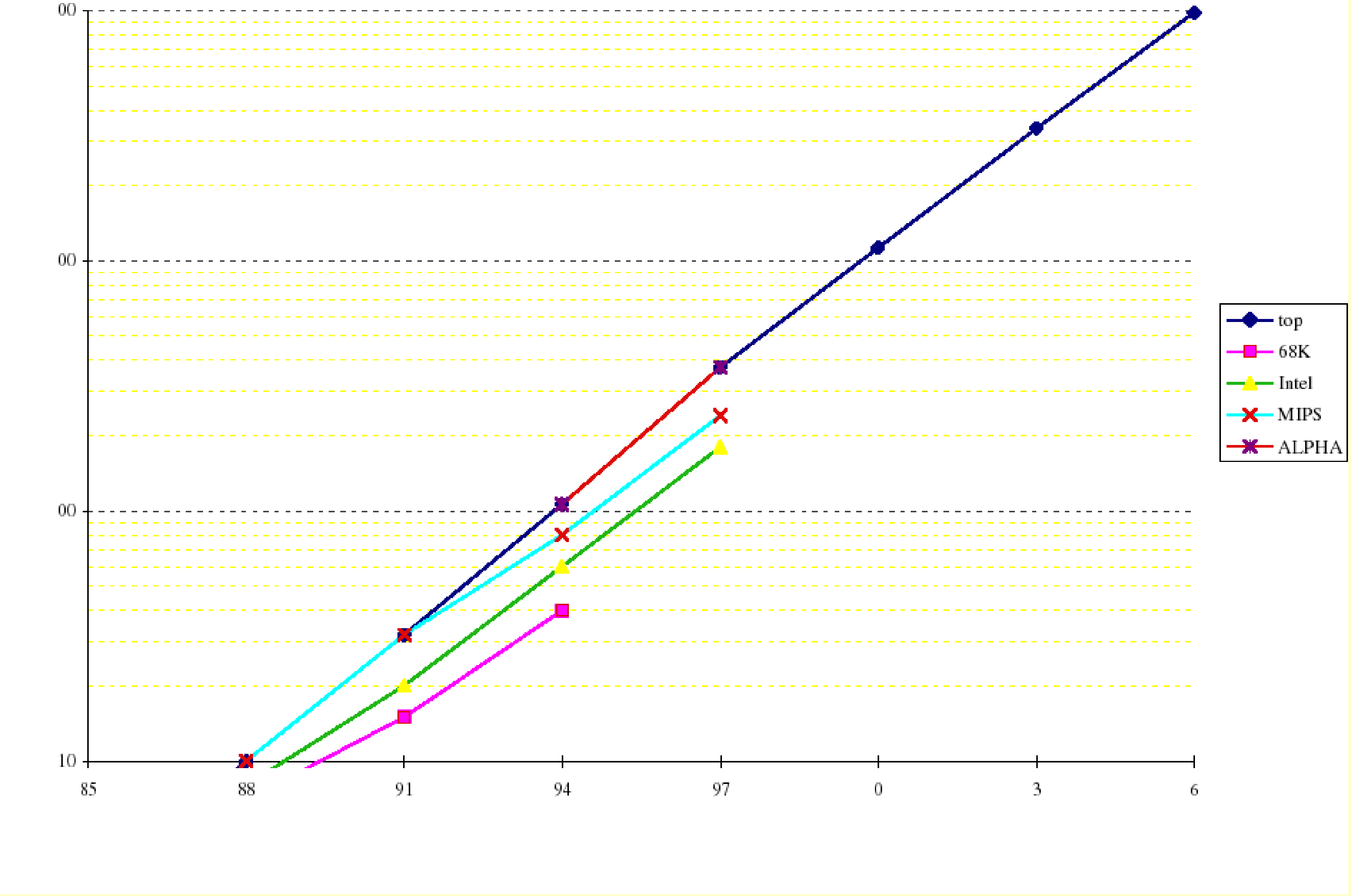
Gbop/s x2.1/y
Gtrans/y x1,8/y
G$/y x1.2/y
$/Gb x0.7/y
10^15
10^12
10^9
10^6
10^3
1
1975
1983
1991
1999
2007

Memories

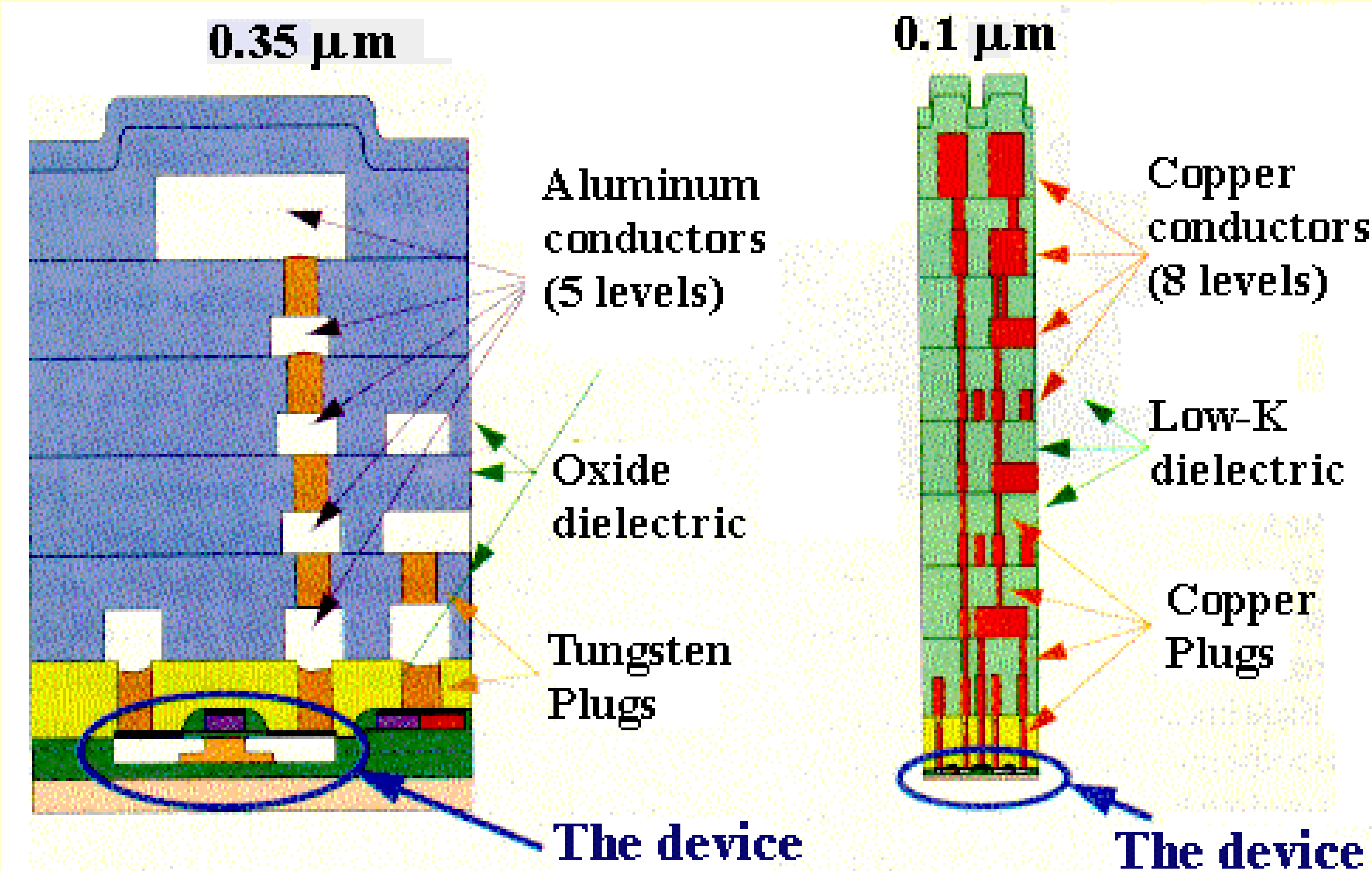


256 Mb
10000
0
10^7
10^5
10^3
10
b/su^2
b/chip
mm^2
MHz
1.6
1.2
1
0.7
0.5
0.35
0.15
Feature size: um.

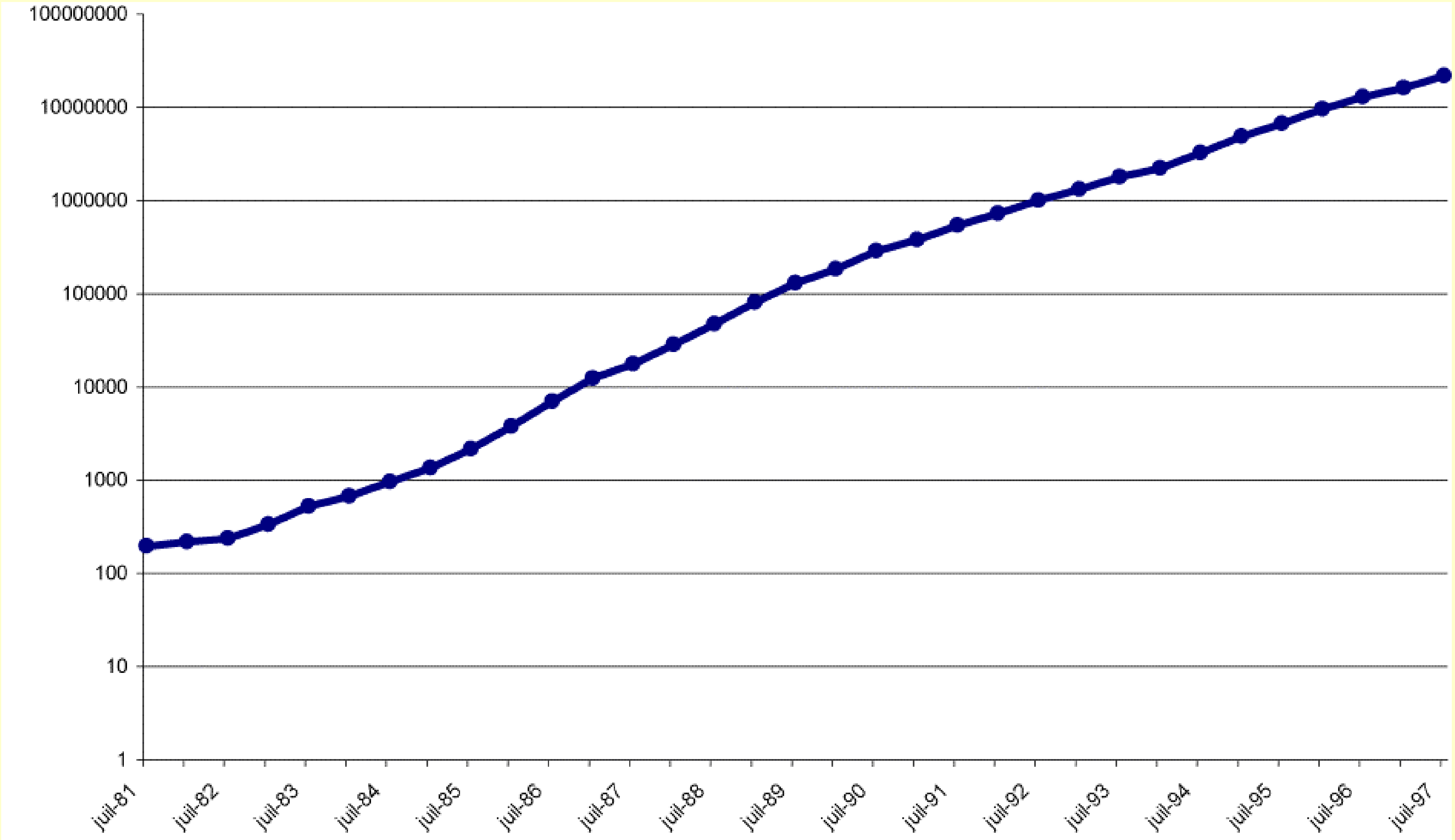
Processors



2007


0.35 µm
0.1 µm
Aluminum conductors (5 levels)
Oxide dielectric
Tungsten Plugs
The device
Copper conductors (8 levels)
Low-K dielectric
Copper Plugs
The device

Internet



100000000
10000000
1000000
100000
10000
1000
100
10
1
juil-81
juil-82
juil-83
juil-84
juil-85
juil-86
juil-87
juil-88
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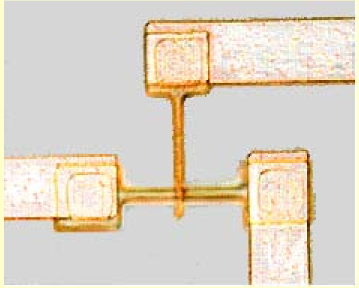
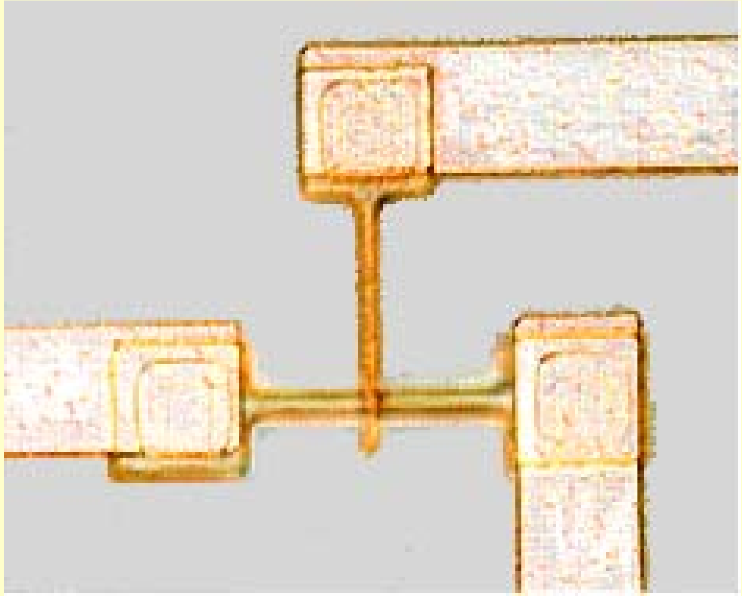
juil-95
juil-96
juil-97

cMOS End Point



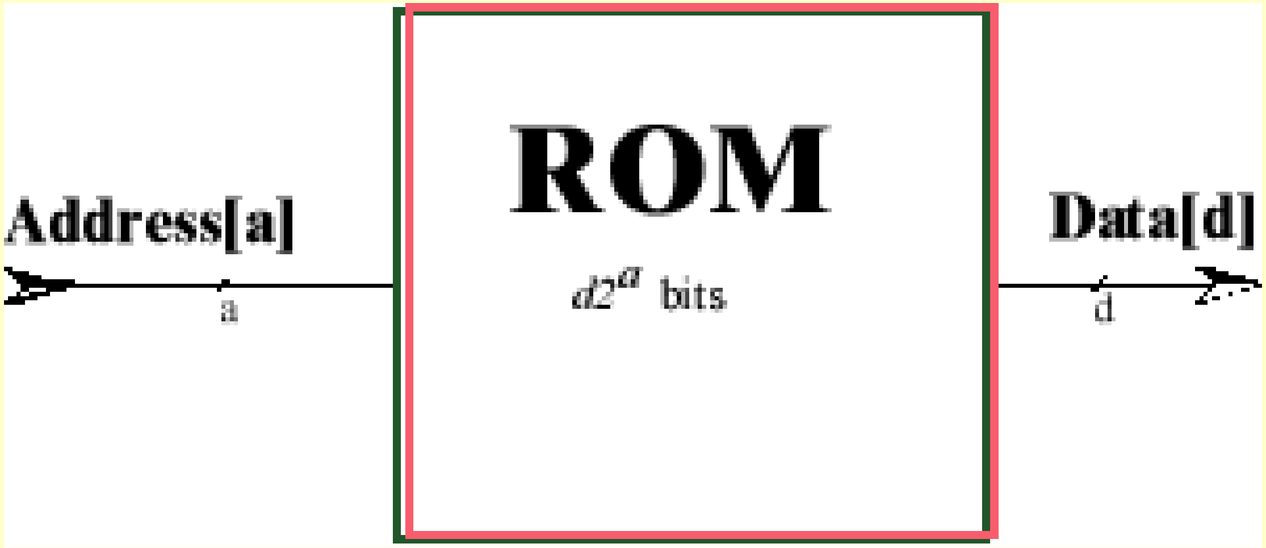


Limits

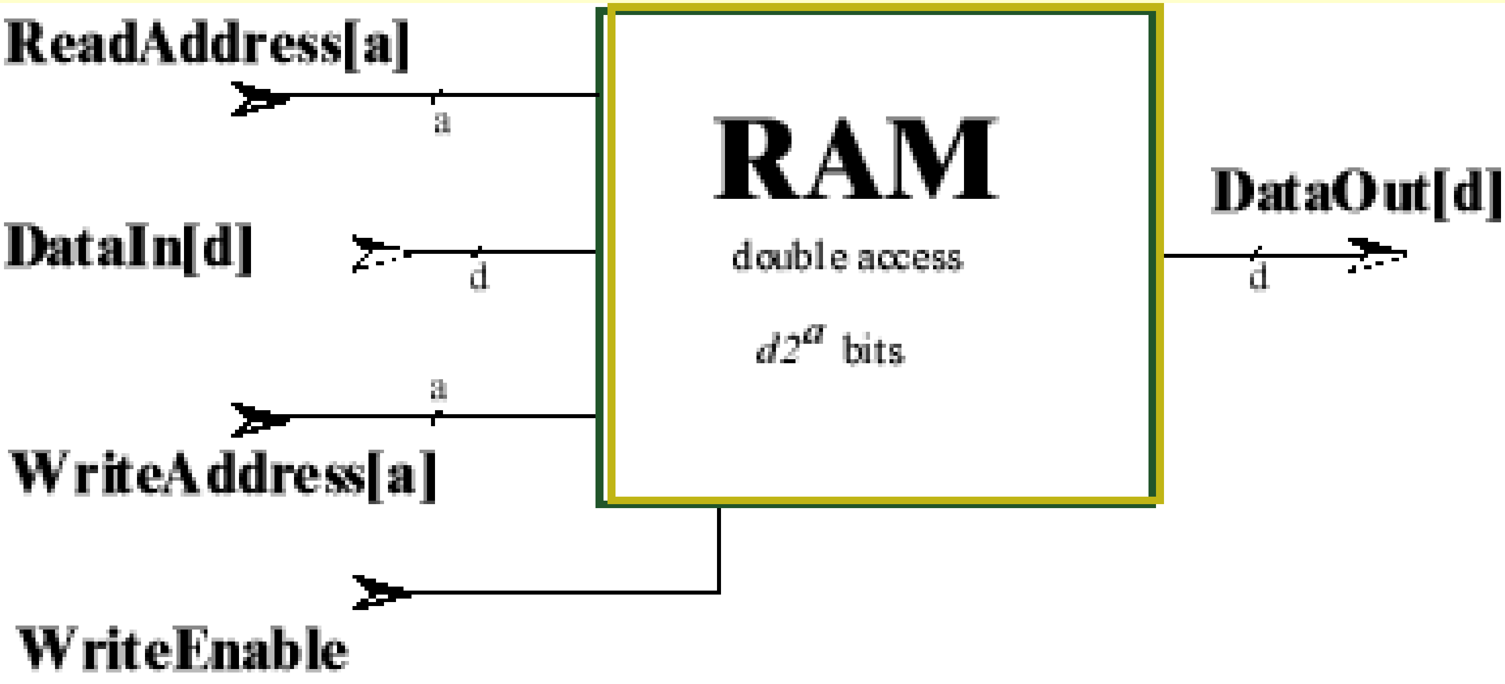
- Physics
- Technology
- Economics

2015?

Memory



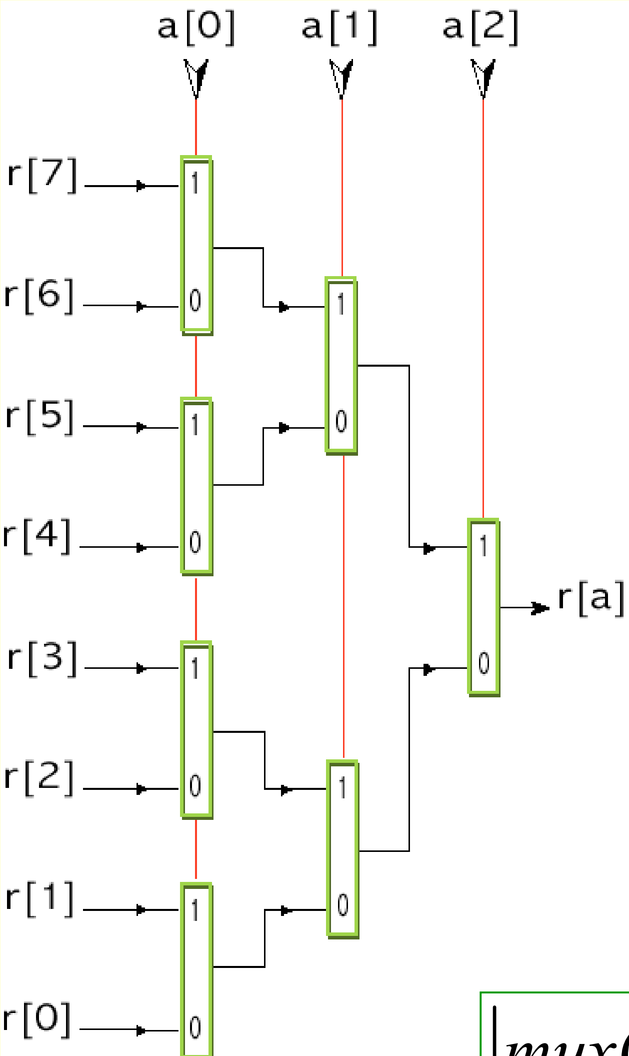
Address[a]
a
ROM
$d2^a$ bits
Data[d]
d

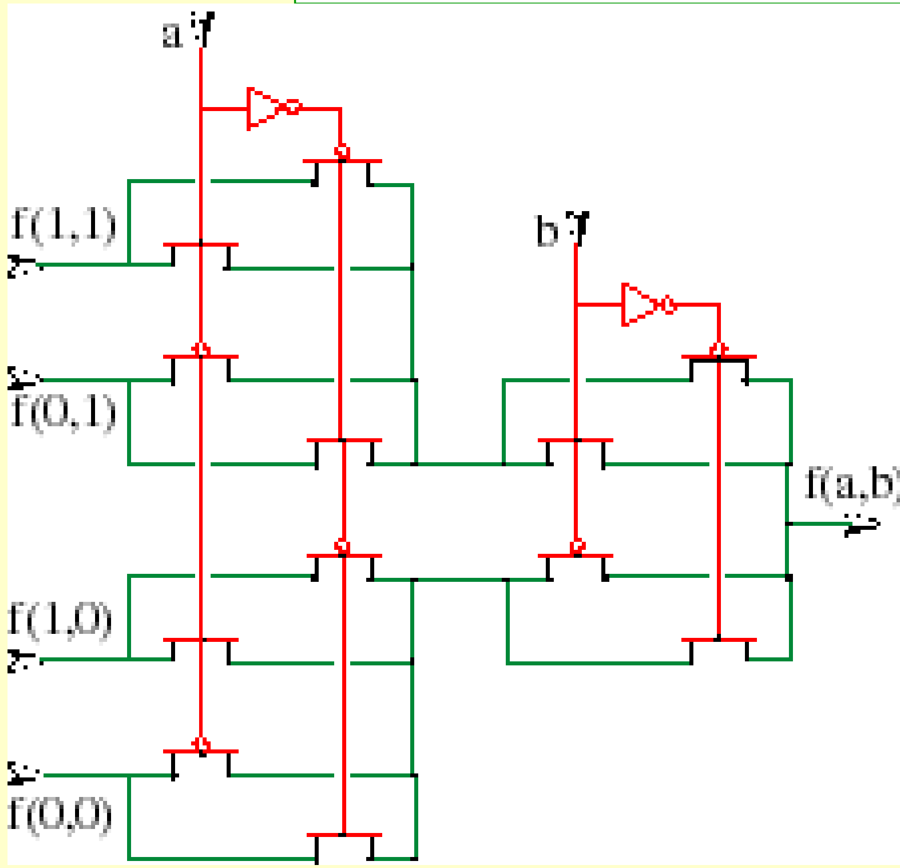


ReadAddress[a]
a
DataIn[d]
d
a
WriteAddress[a]
WriteEnable
RAM
double access
$d2^a$ bits
DataOut[d]
d

2^N ways MUX

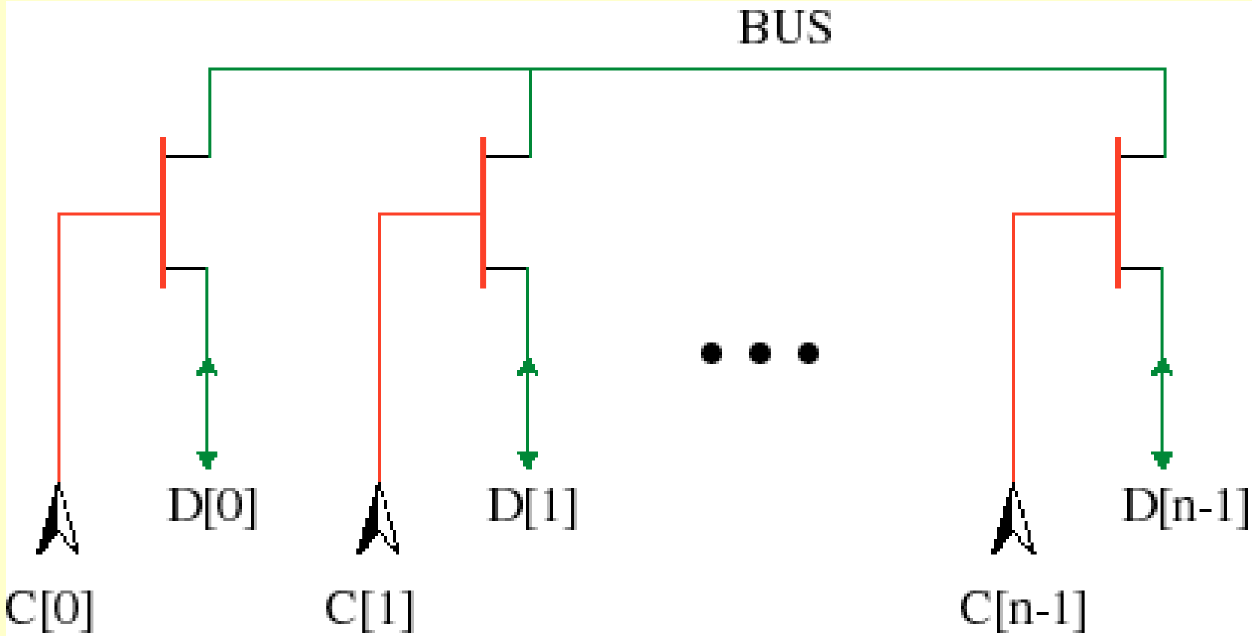
$$|mux(2^N)| \quad = \quad N2^N$$

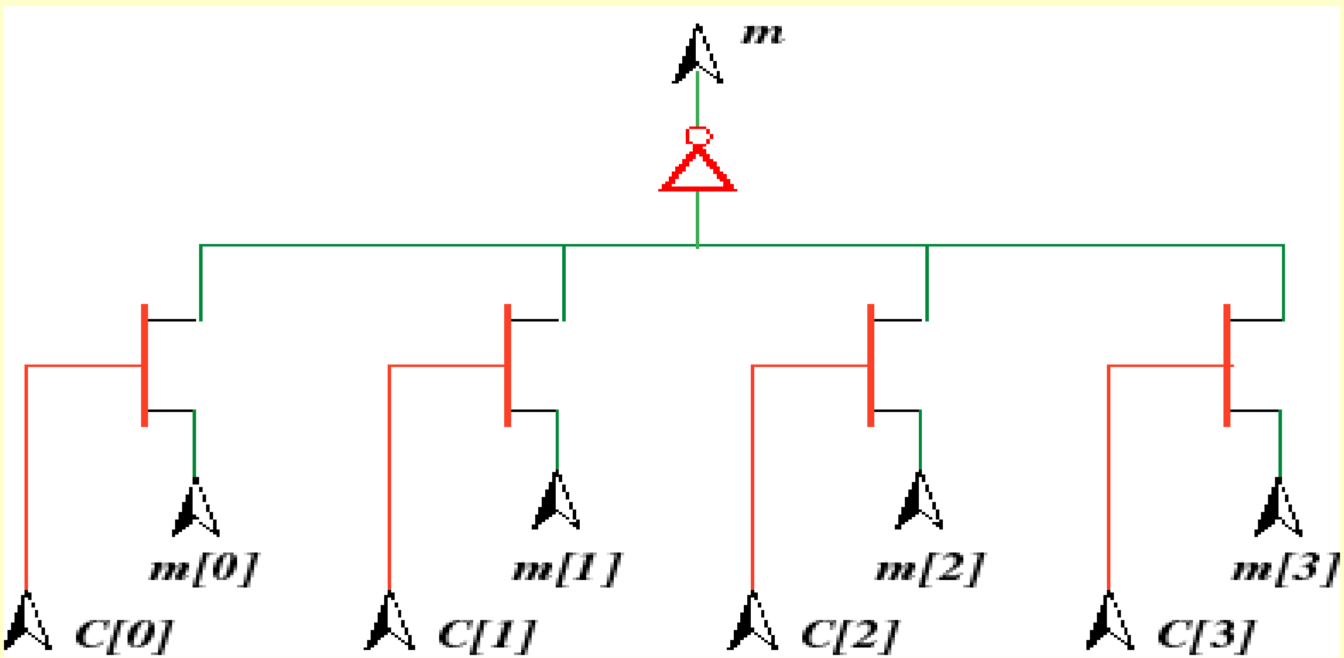




$$|mux(2^N)| \quad = \quad \max\left\{(2^N-1)|mux|, \quad N2^N|wire|\right\}$$

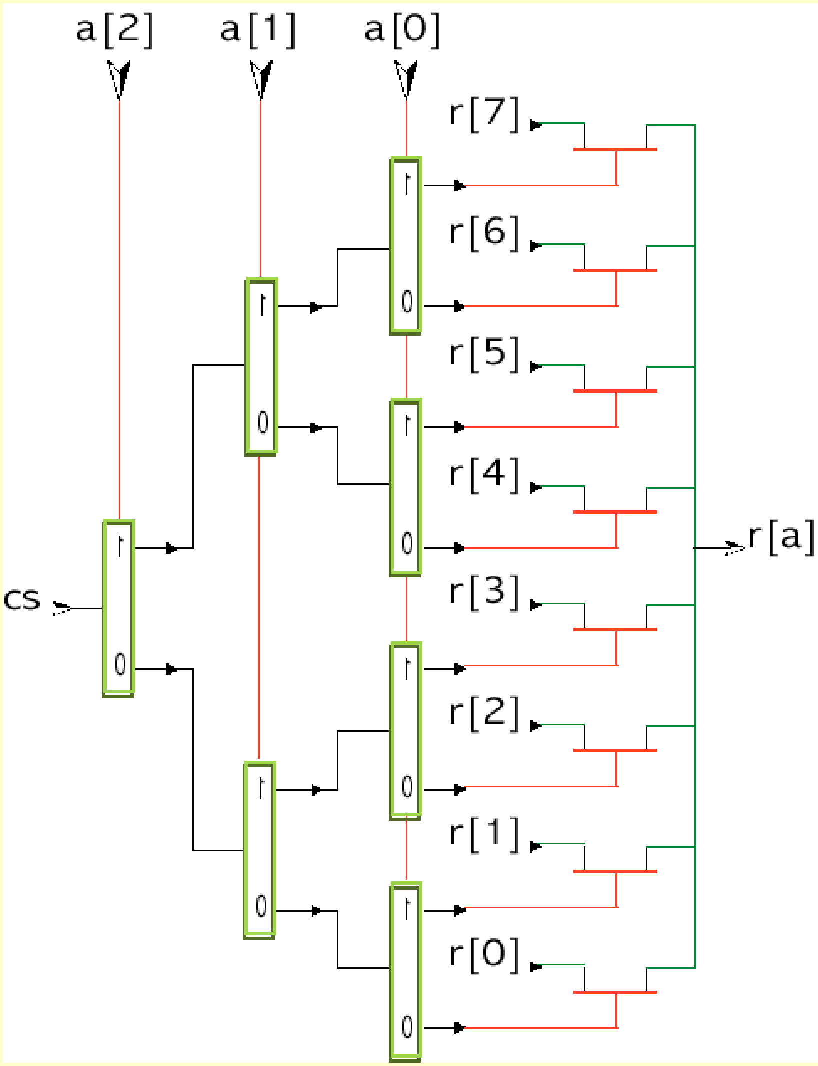
Bus

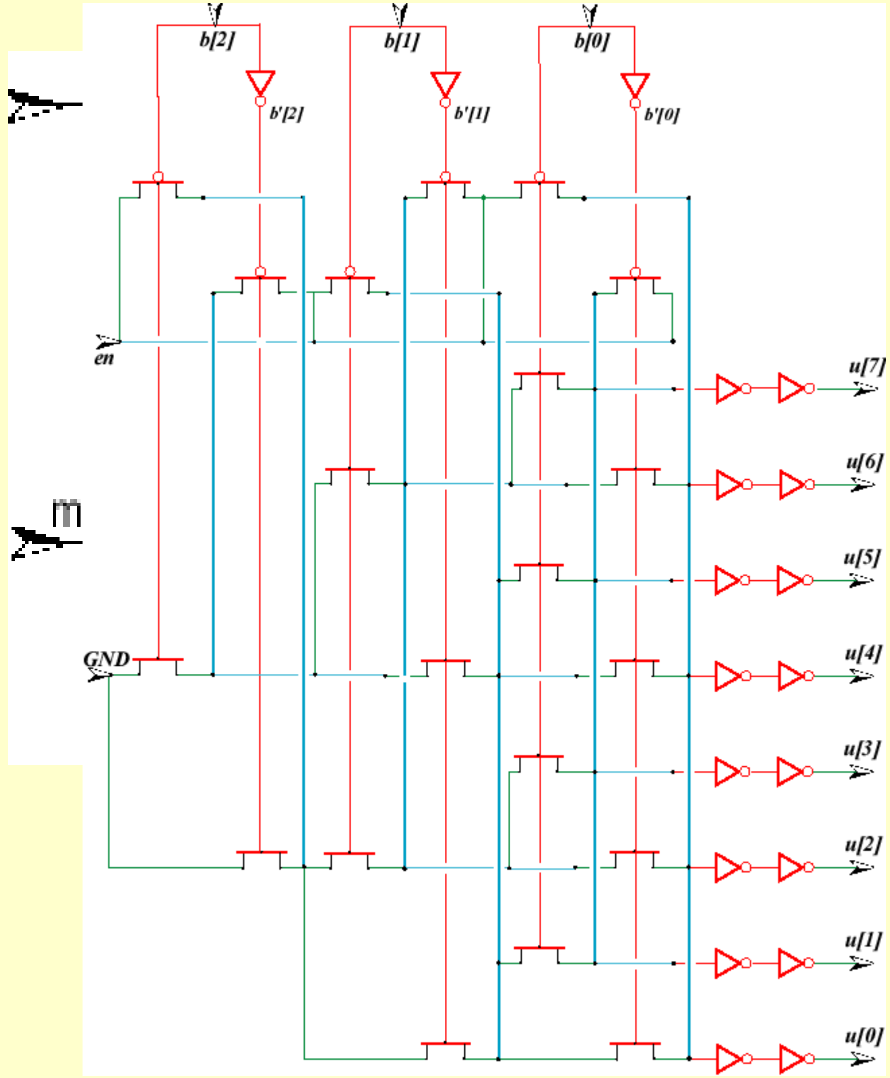




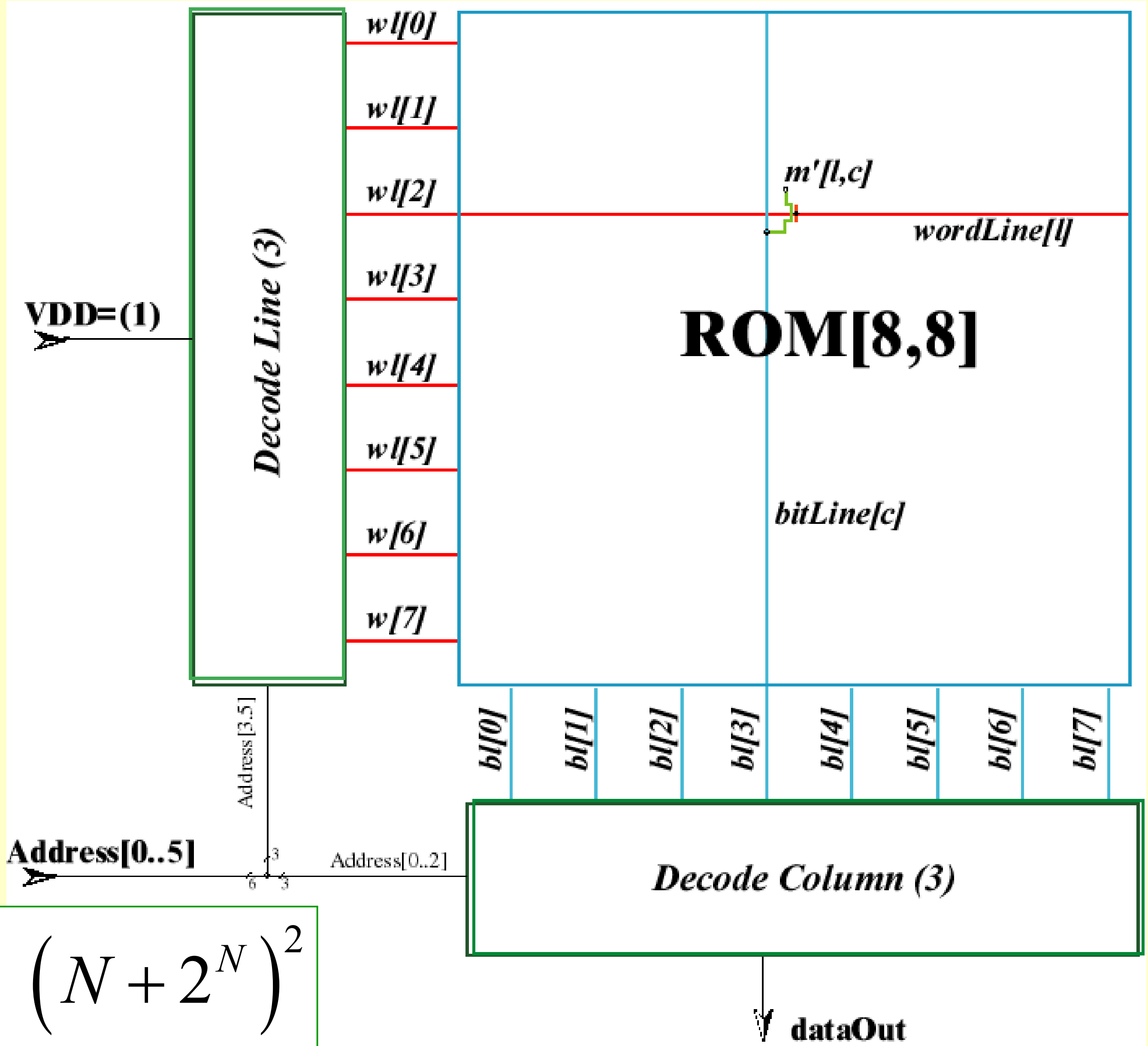
2^N ways deMUX

$$\left| demux(2^N) \right| = N2^N$$





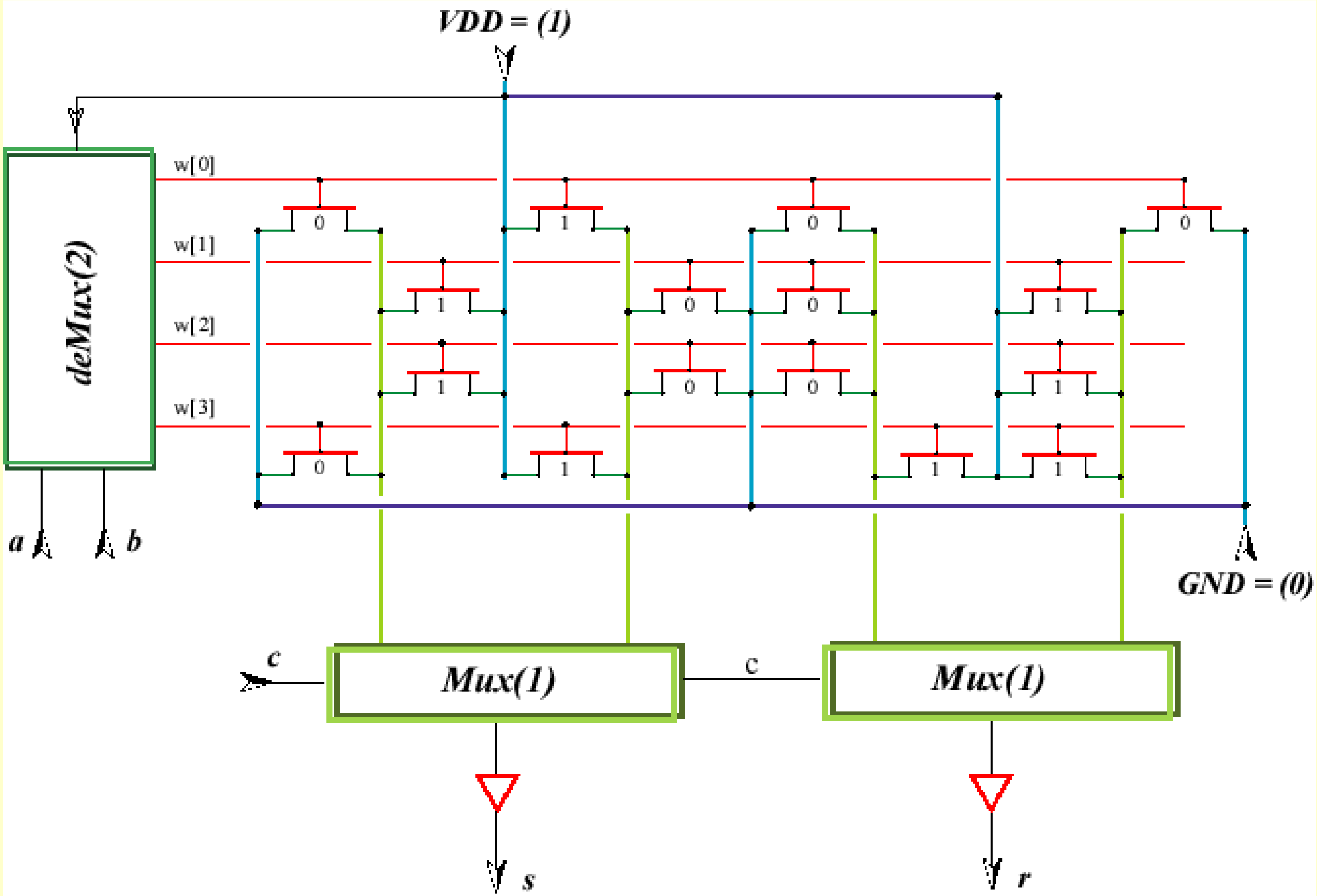
ROM



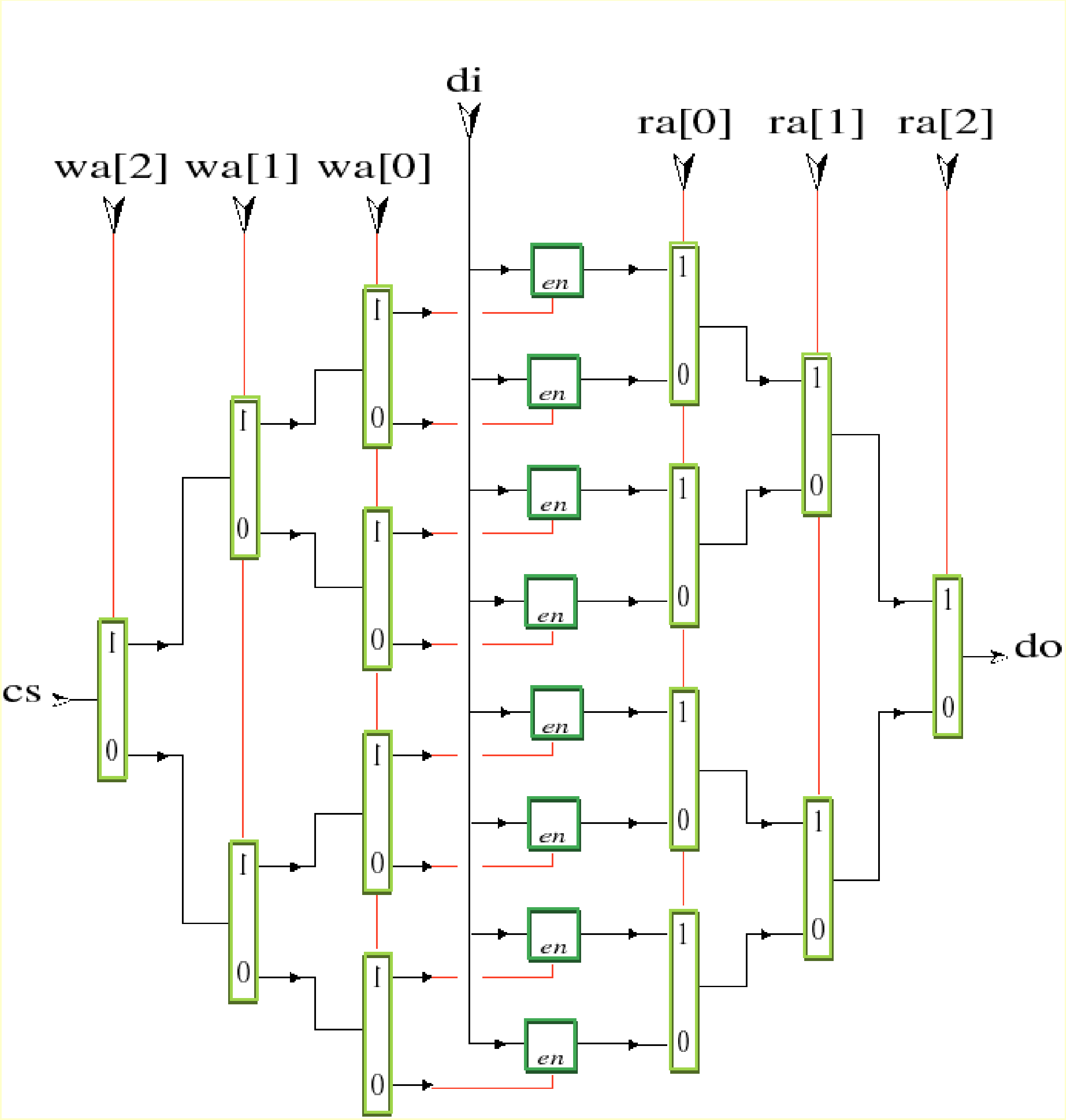
$$\left|ROM(2^{2N})\right| = \left(N + 2^N\right)^2$$

$$= 2^{2N} + N2^{N+1} + N^2$$

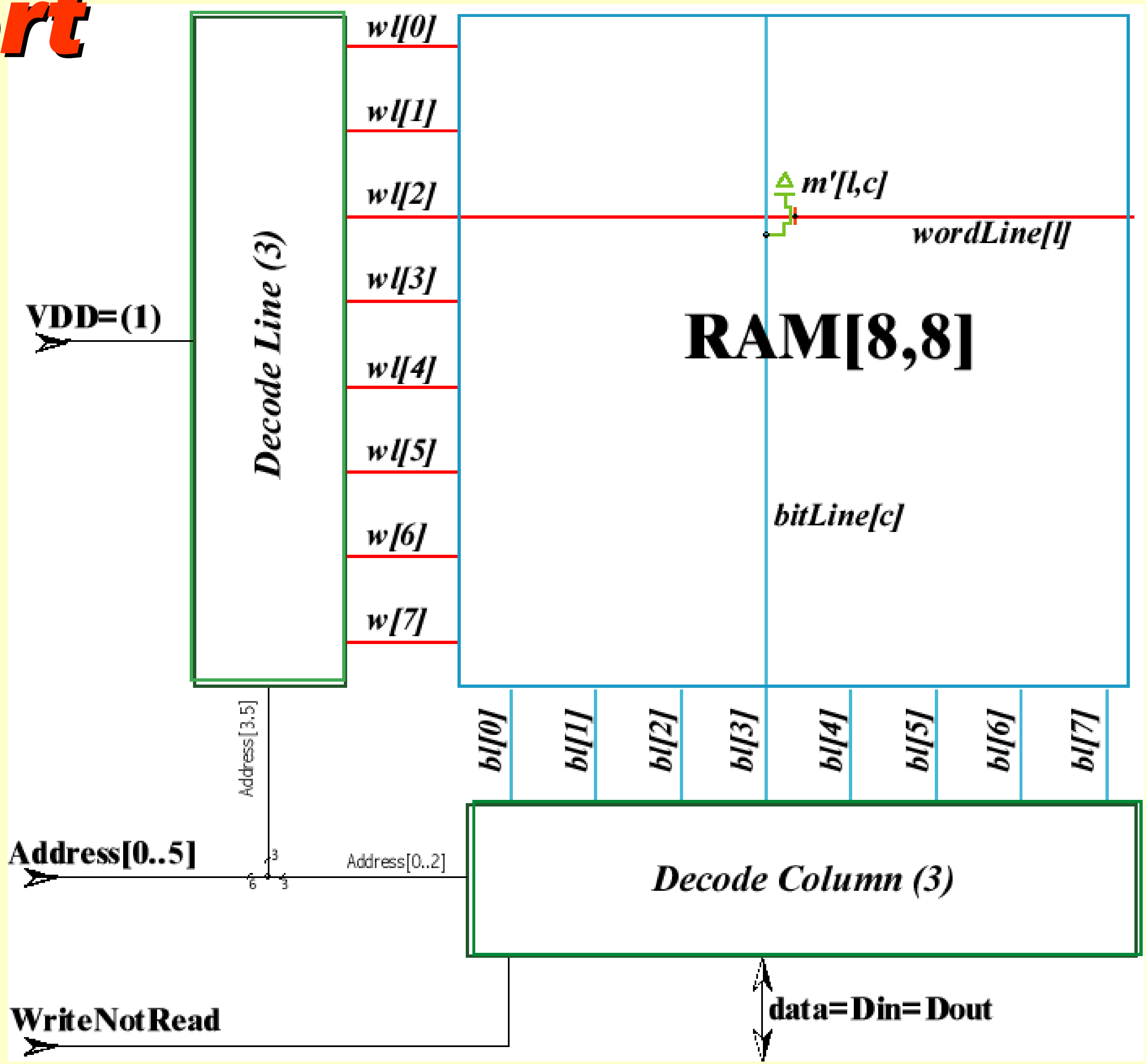
ROM: Full Adder



Dual Port Memory



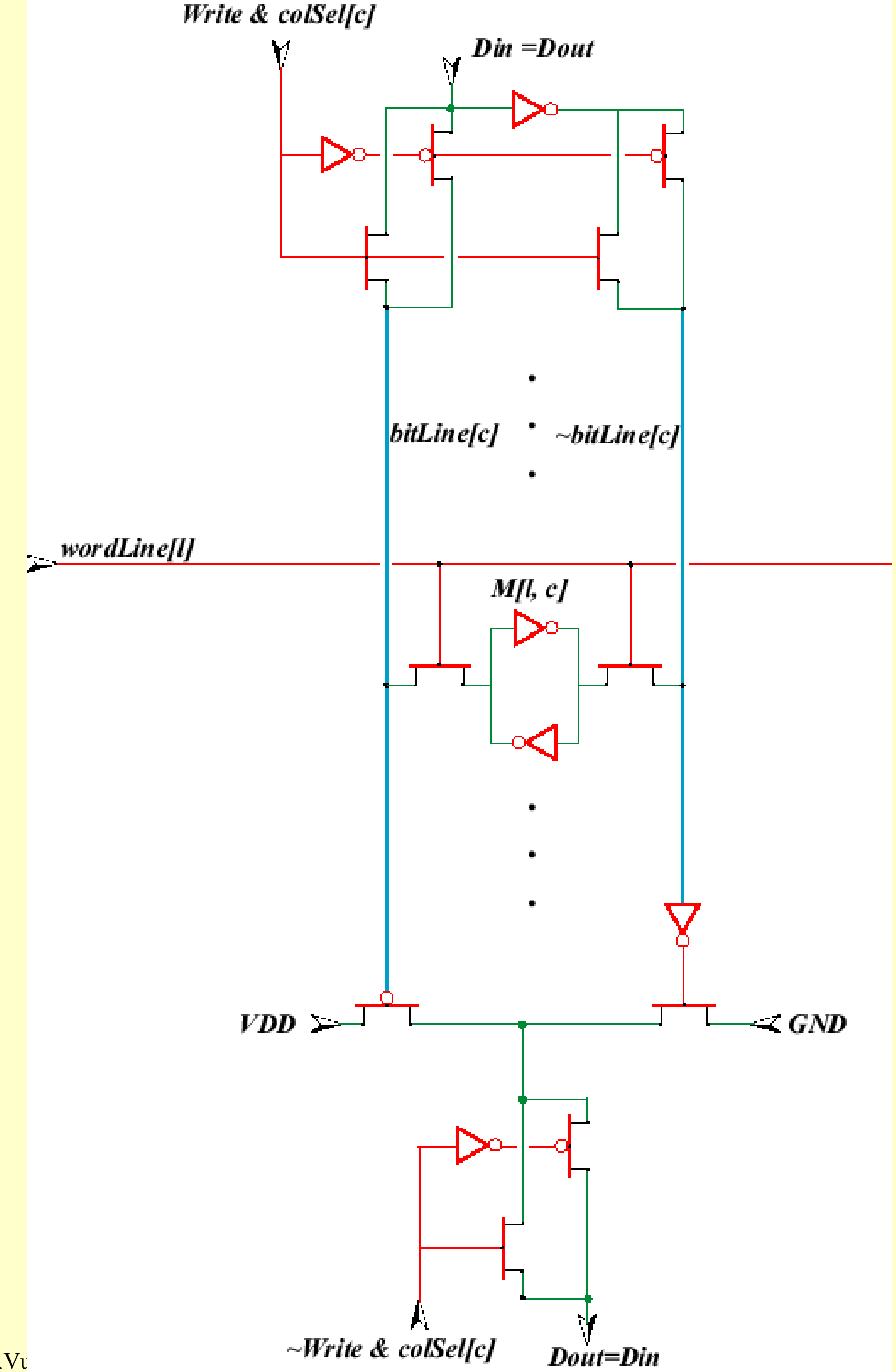
Single Port Memory



sRAM

6 transistors/bit

5 transistors/bit



dRAM

1 transistor/bit

1/2 transistor/bit